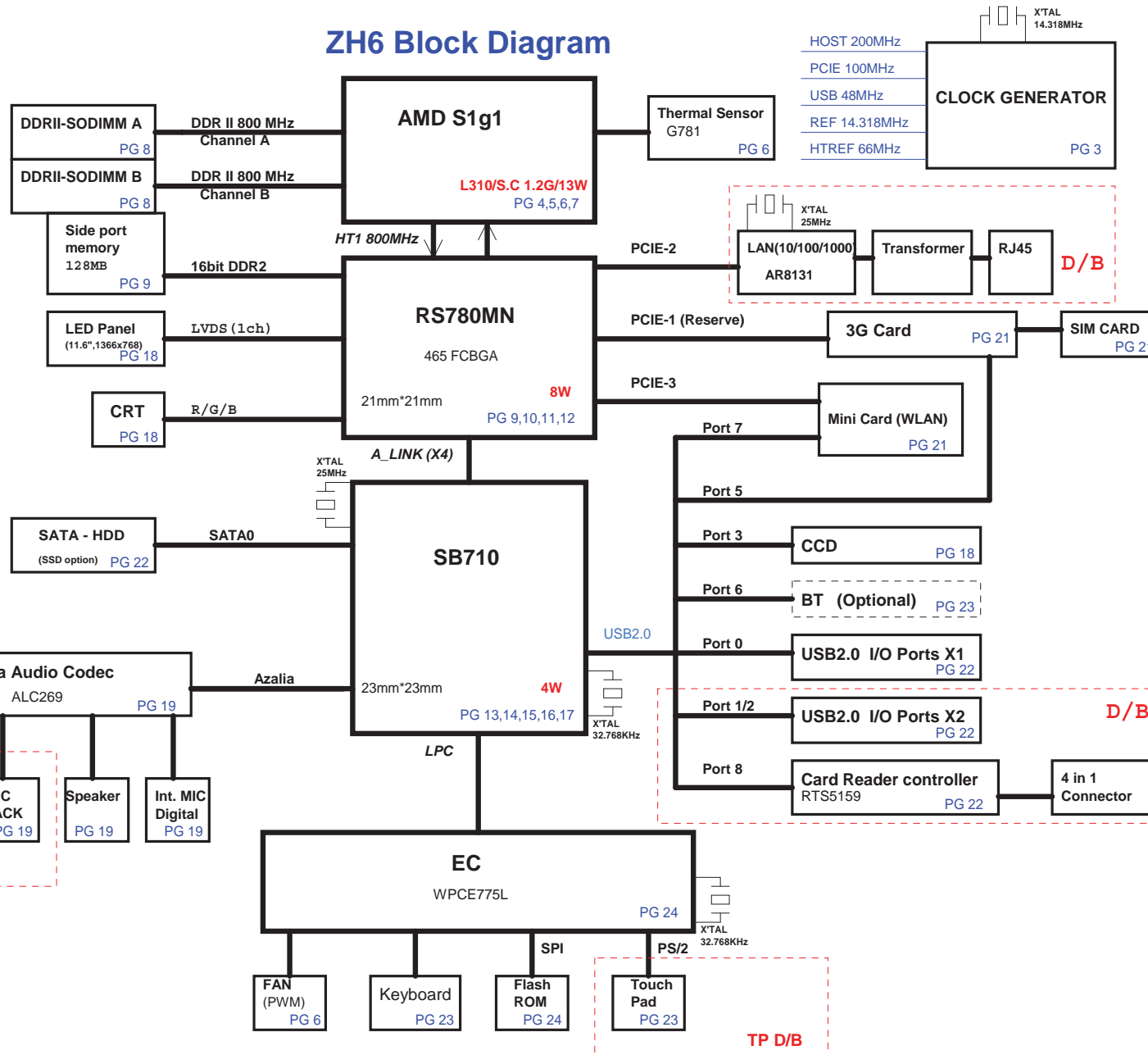
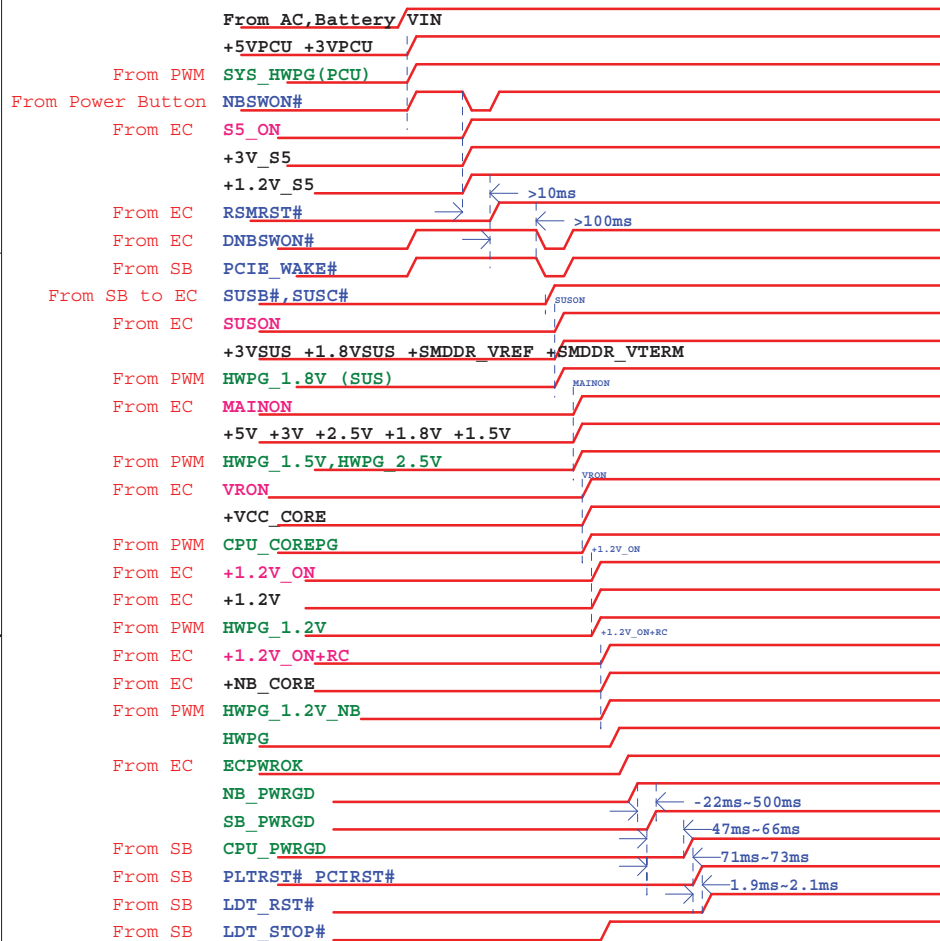


# ZH6 Block Diagram



## ZH6 Power On Sequence



\*Note: EC will sampling SUSB# & SUSC# every 5ms.

## AMD SB710 SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
SB710 SDATA0/SCLK0 (+3V)	V	V	V
SB710 SDATA1/SCLK1 (+3V_S5)			
Power Plane	+3V	+3V	+3V
MOS CKT	Reserve	Reserve	Reserve

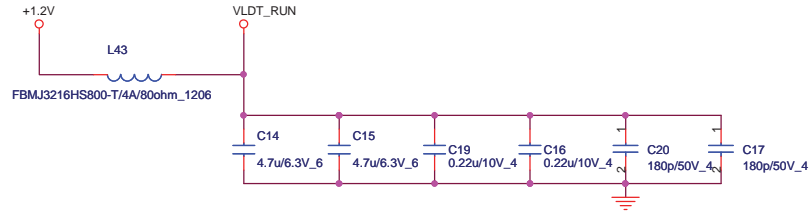
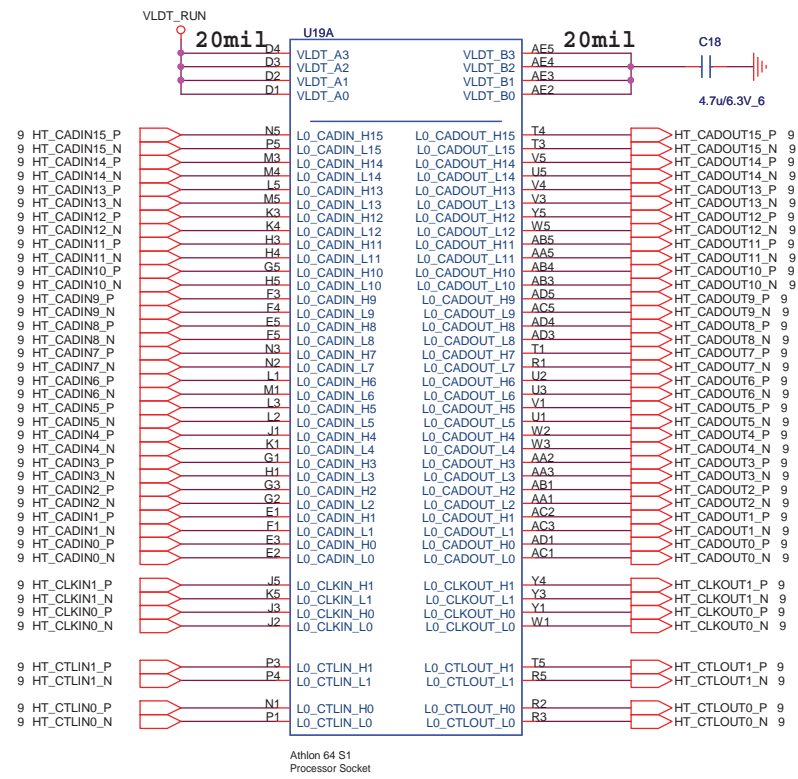
## BOM naming rule

Items	Function	Name	Description
1	3G Module	3G@	
2	HDT debug function	HDT@	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			


## EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDATA1/SCLK1 (+3VPCU)	V		
EC775 SDATA2/SCLK2 (+3VPCU)		V	
EC775 SDATA3/SCLK3 (+3VPCU)			V
EC775 SDATA4/SCLK4 (+3VPCU)			
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	X	X





Power name	Description	Voltage
VLDT_A/B	HyperTransport I/O ring power supply	1.2V



Quanta Computer Inc.

PROJECT : ZH6

TURION 64 HT I/F

Size	Document Number	Rev 1A
Date:	Monday, August 24, 2009	Sheet 4 of 33

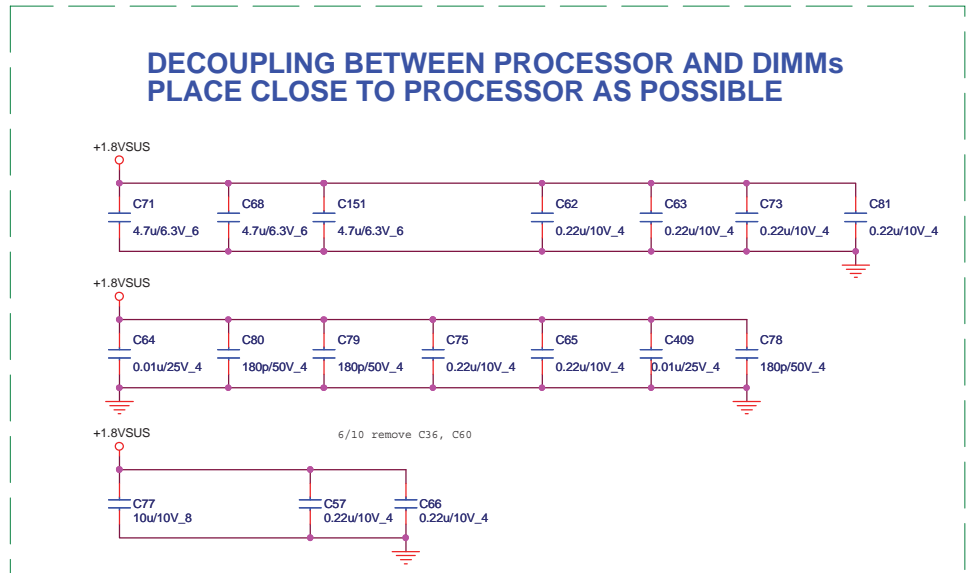
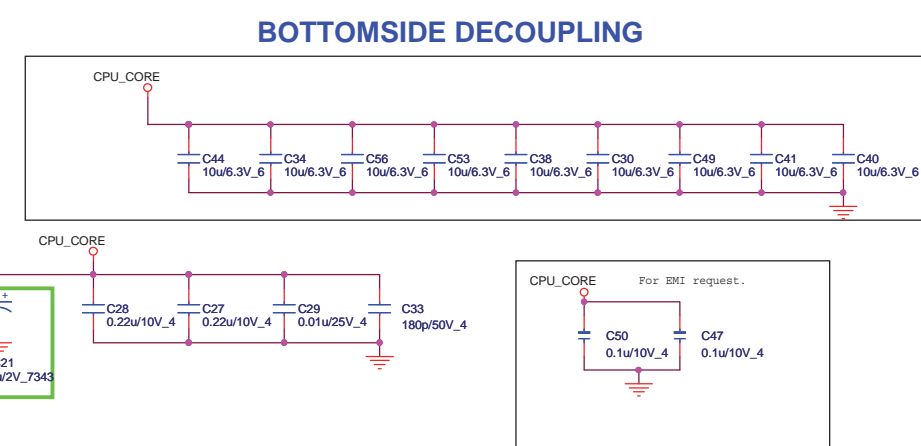
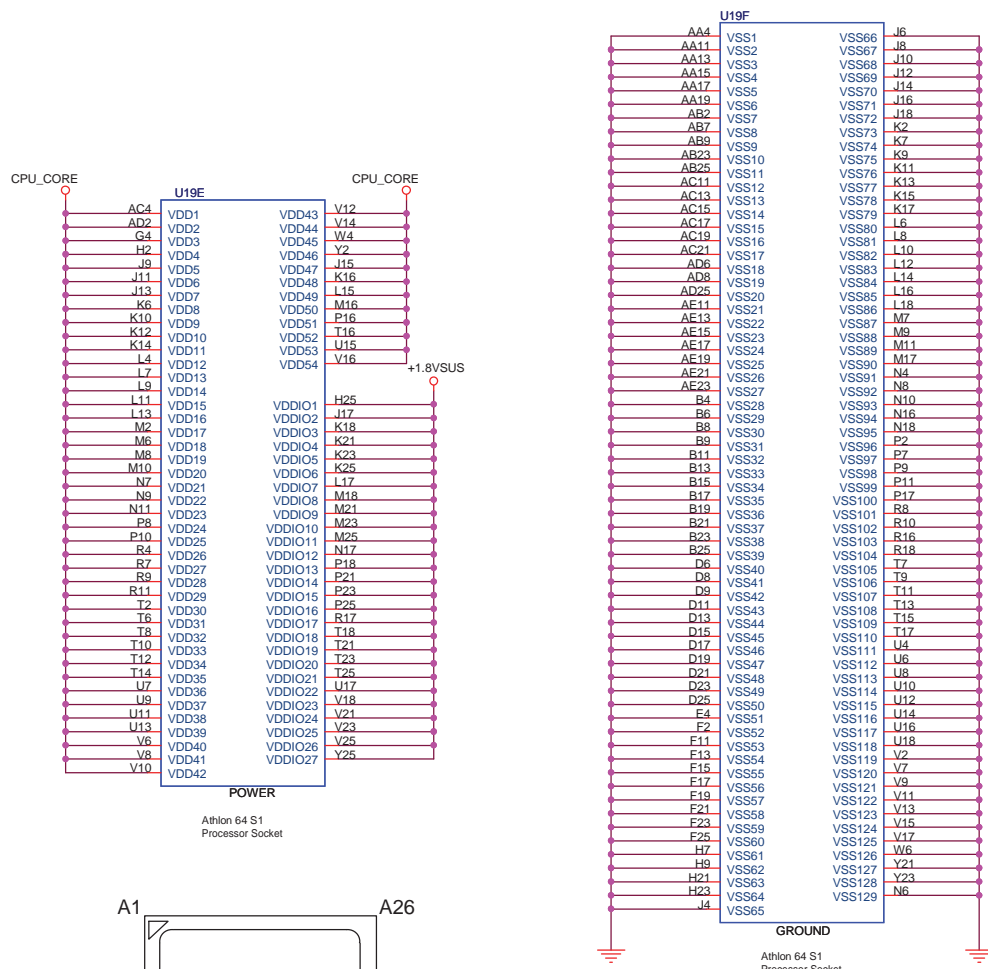
## Processor DDR2 Memory Interface




Power name	Description	Voltage
VTT	VTT Power	0.9V



PROCESSOR POWER AND GROUND(CPU)



Power name	Description	Voltage
VDD	Core power supply	1.05V
VDDIO	DDR SDRAM I/O ring power supply	1.8V



Quanta Computer Inc.

PROJECT : ZH6

TURION 64 PWR & GND

Size

Document Number

Date: Monday, August 24, 2009

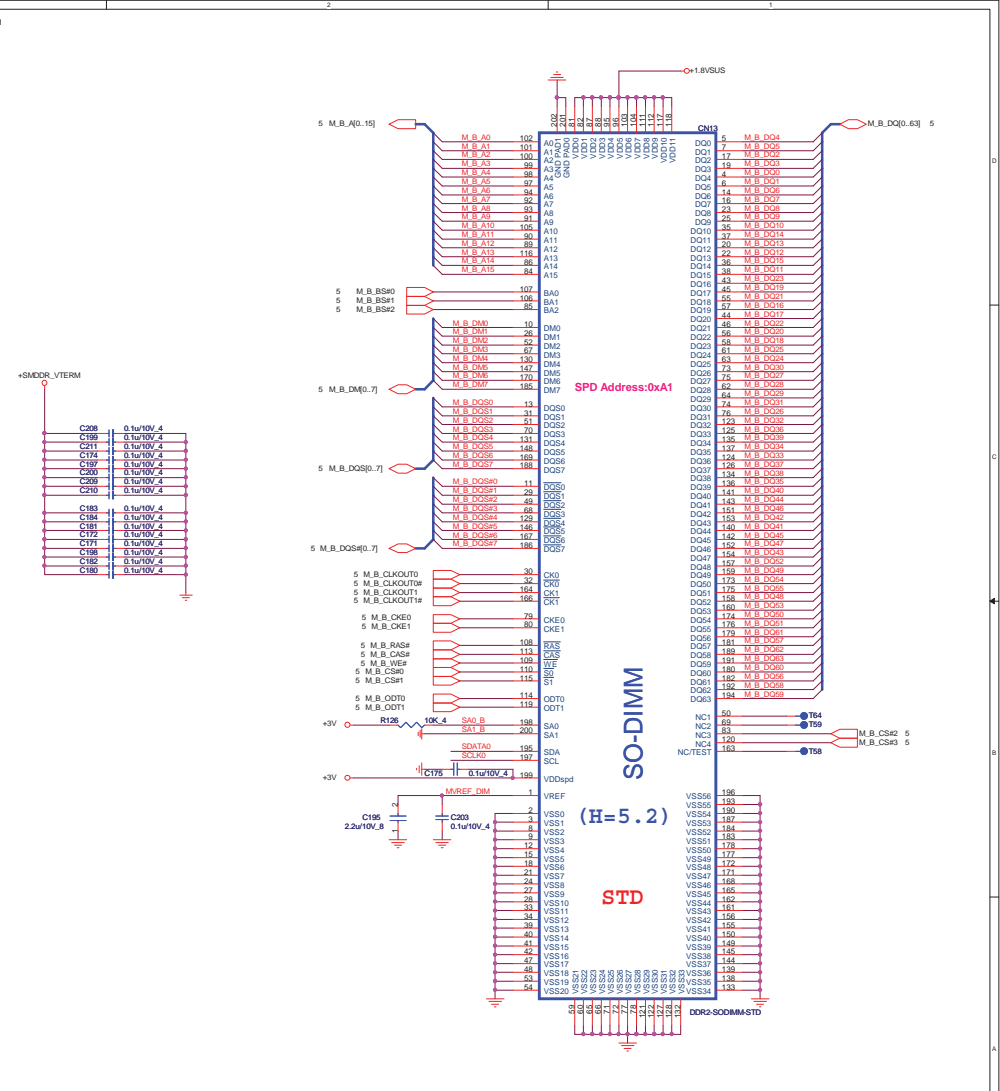
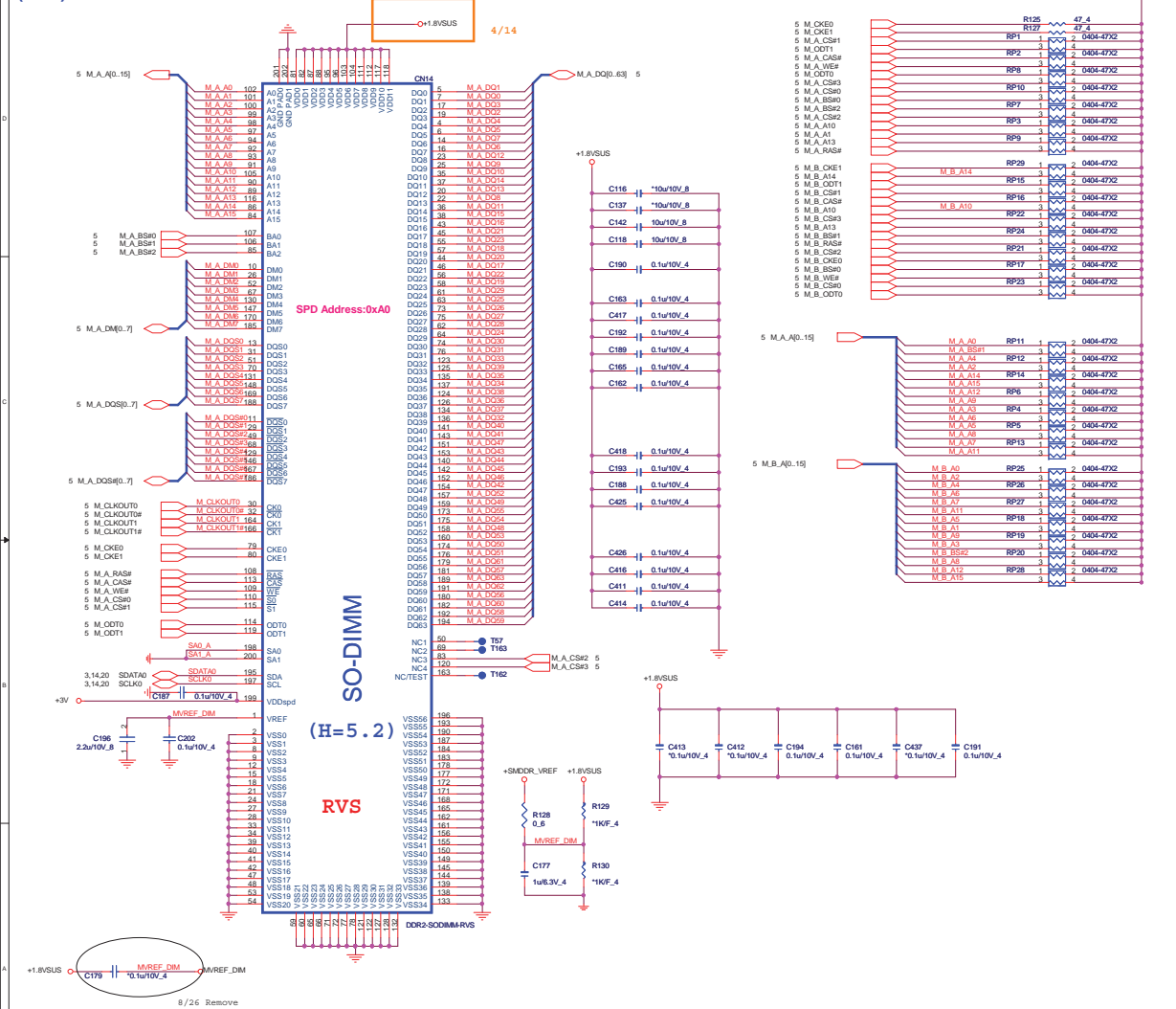
Rev

1A

Sheet 7 of 33

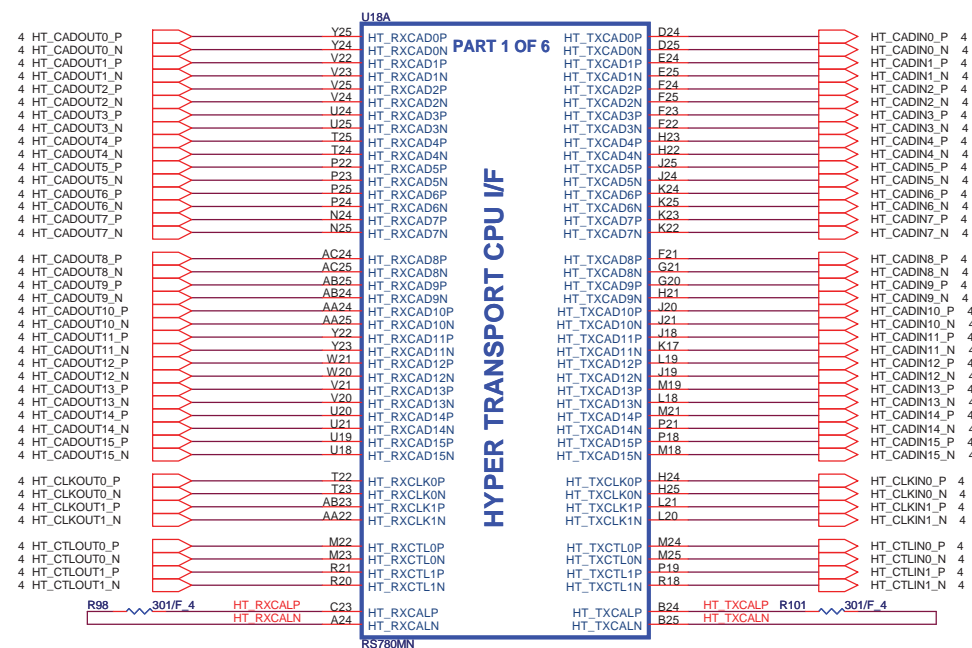


(DDR)





## RS780(CLG)



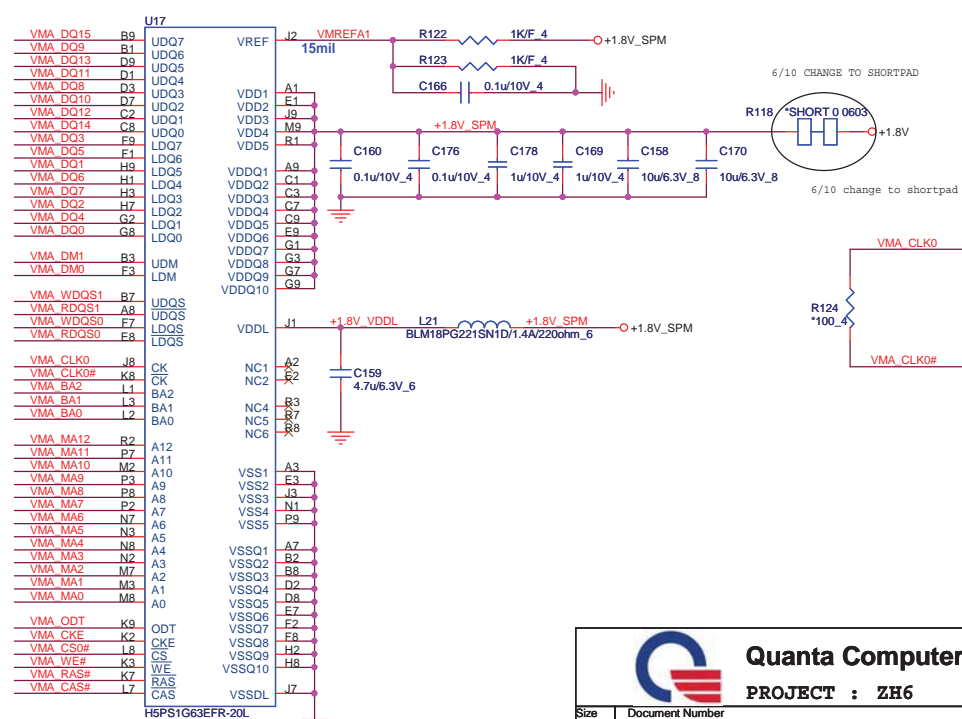
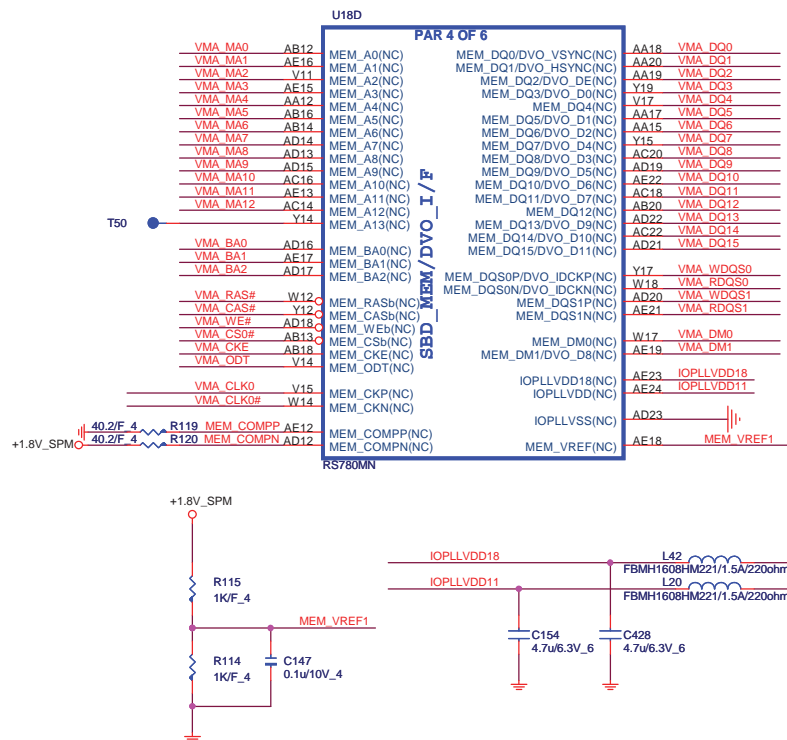
signals	RS780	RX780
HT_TXCALP	R2364 301 ohm 1%	R2364 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R2365 301 ohm 1%	R2365 1.21k ohm 1%
HT_RXCALN		

## RS780(CLG)

**SIDE-PORT Reserved**

**This block is for UMA RS780 only , RX780 NC**

## SPM(CLG)



**Quanta Computer Inc.**

PROJECT : ZH6

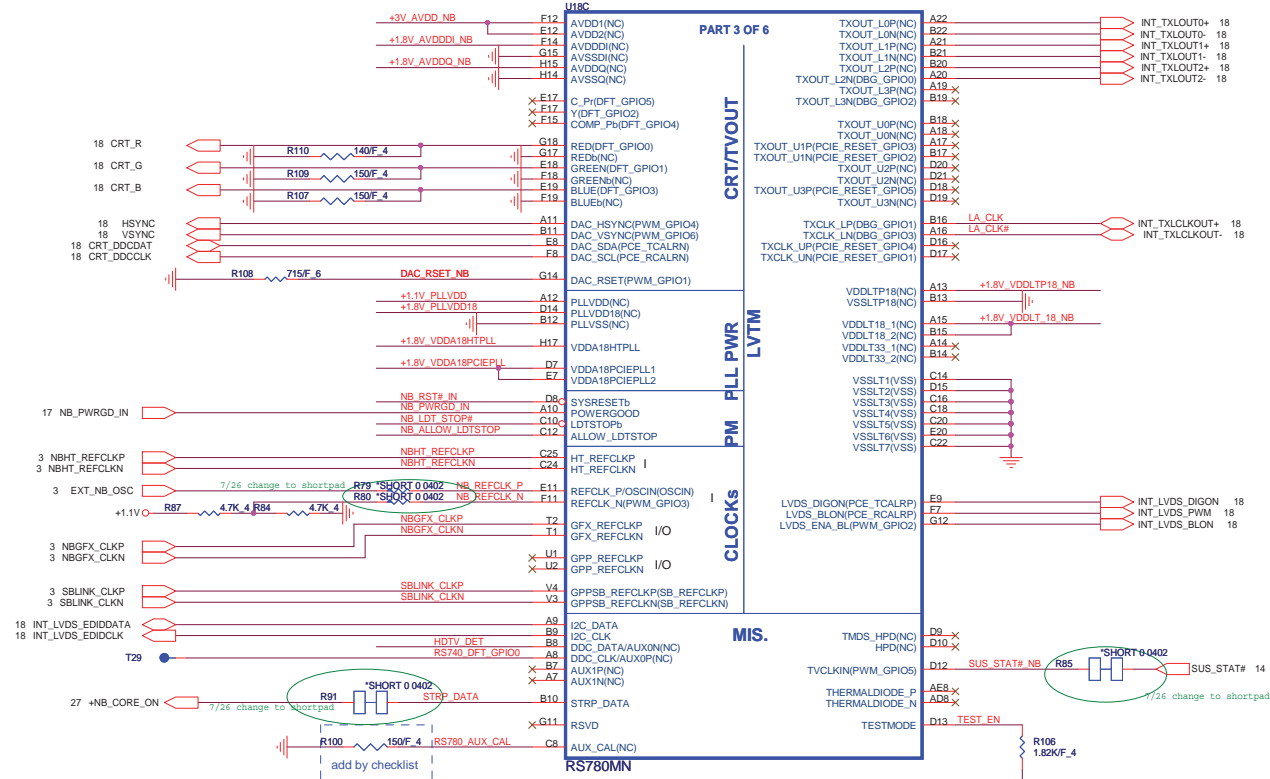
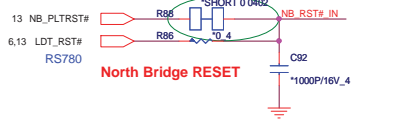
Size	Document Number	Rev
	<b>RS780MN-HT LINK I/F 1/4</b>	1A
Date:	Monday, August 24, 2009	Sheet 9 of 33



RS780(CLG)

RX780: Powered from the 1.8-V rail and driven by SB600 LDT\_RST#, or SB700 LDT\_RST# or A\_RST#.

RS780: Powered from the 3.3-V rail and driven by SB600 LDT\_RST#, or SB700 LDT\_RST# or A\_RST#.



Enables Debug Bus access through memory T/O pads and GPIO.

0: Enable RS780, Default

1: Disable RS780 (RS780 use VSYNC#)

VSYNC

R97

3K\_4

+3V

Indicates if memory Side port is available or not

0: available RS780, Default

1: Not available RS780 (RS780 use HSYNC#)

HSYNC

R99

3K\_4

+3V

R102

3K\_4

For external EEPROM Debug only

STRP\_DATA

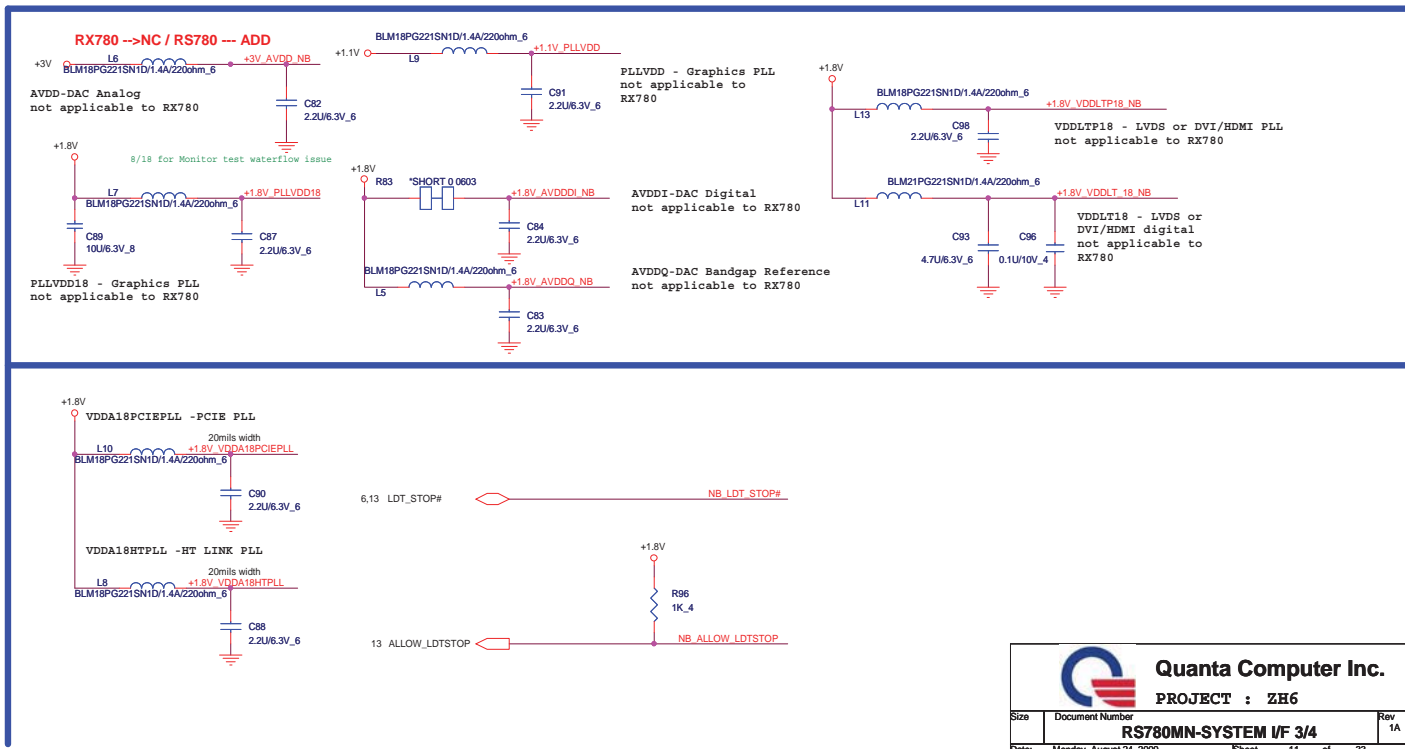
R95

10K/F\_4

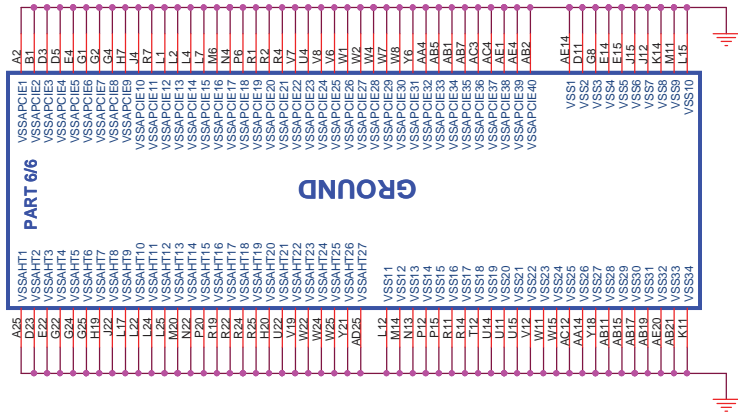
+3V

R94

10K/F\_4

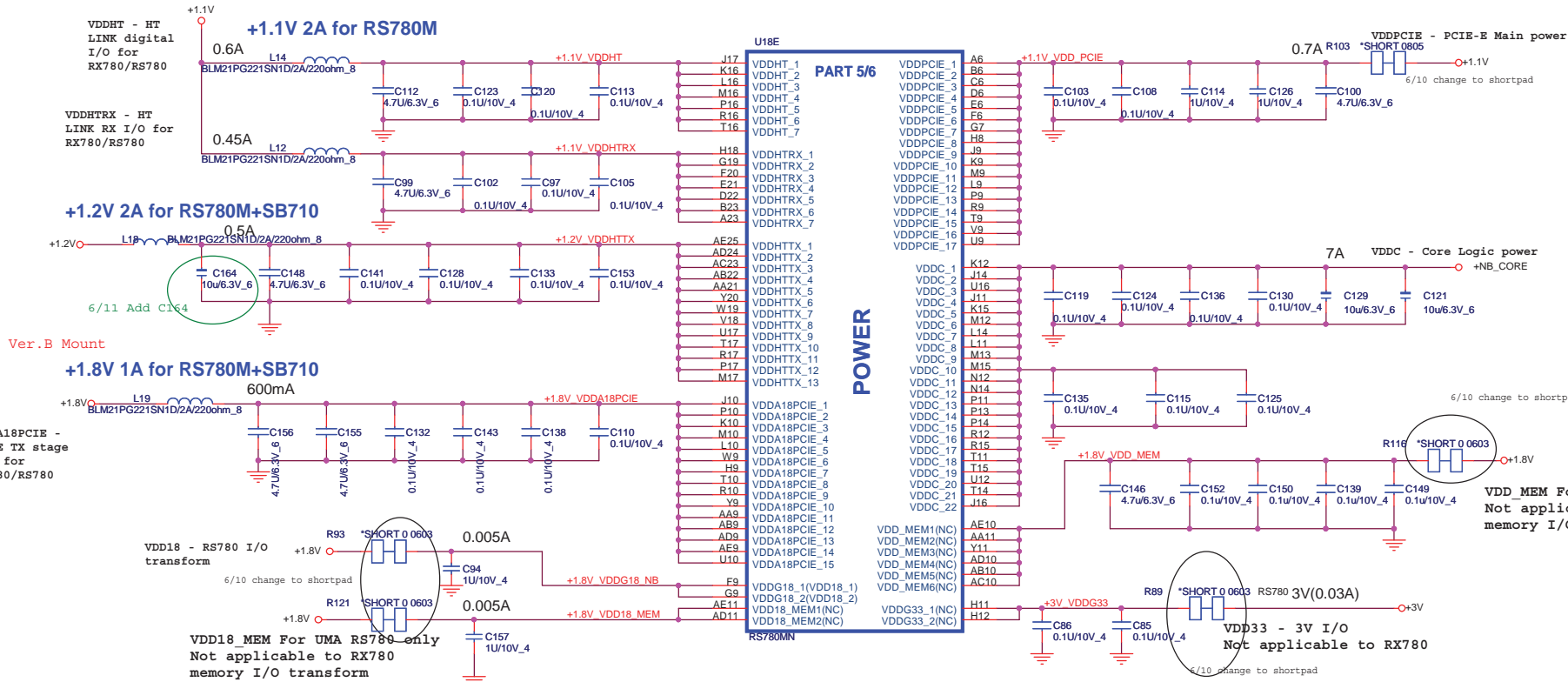


U18F

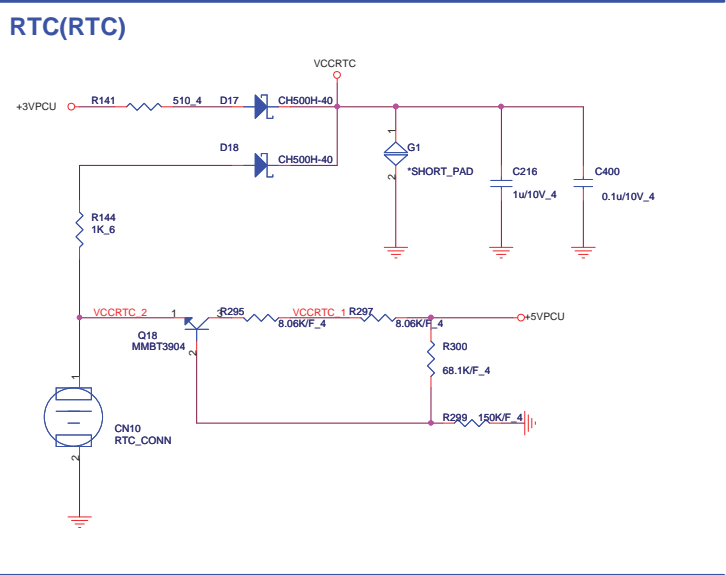
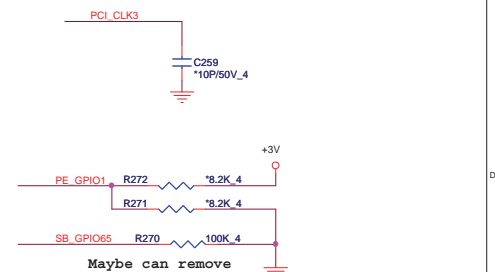


RX780/RS780 POWER DIFFERENCE TABLE

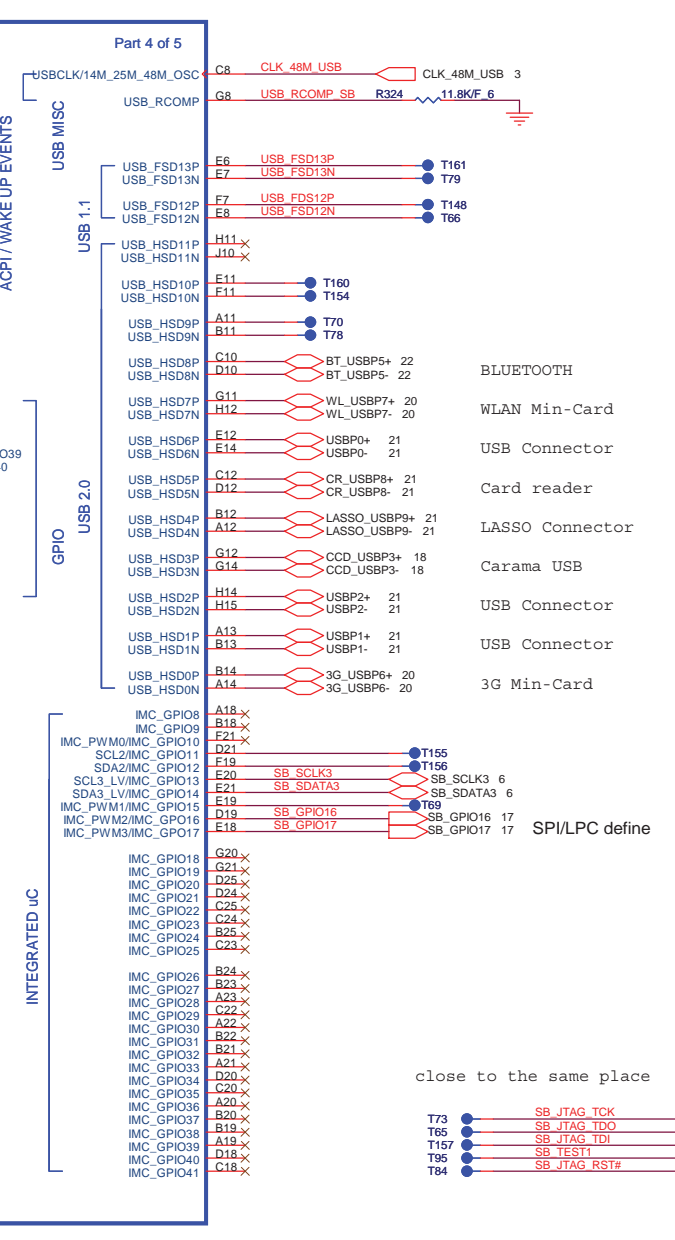
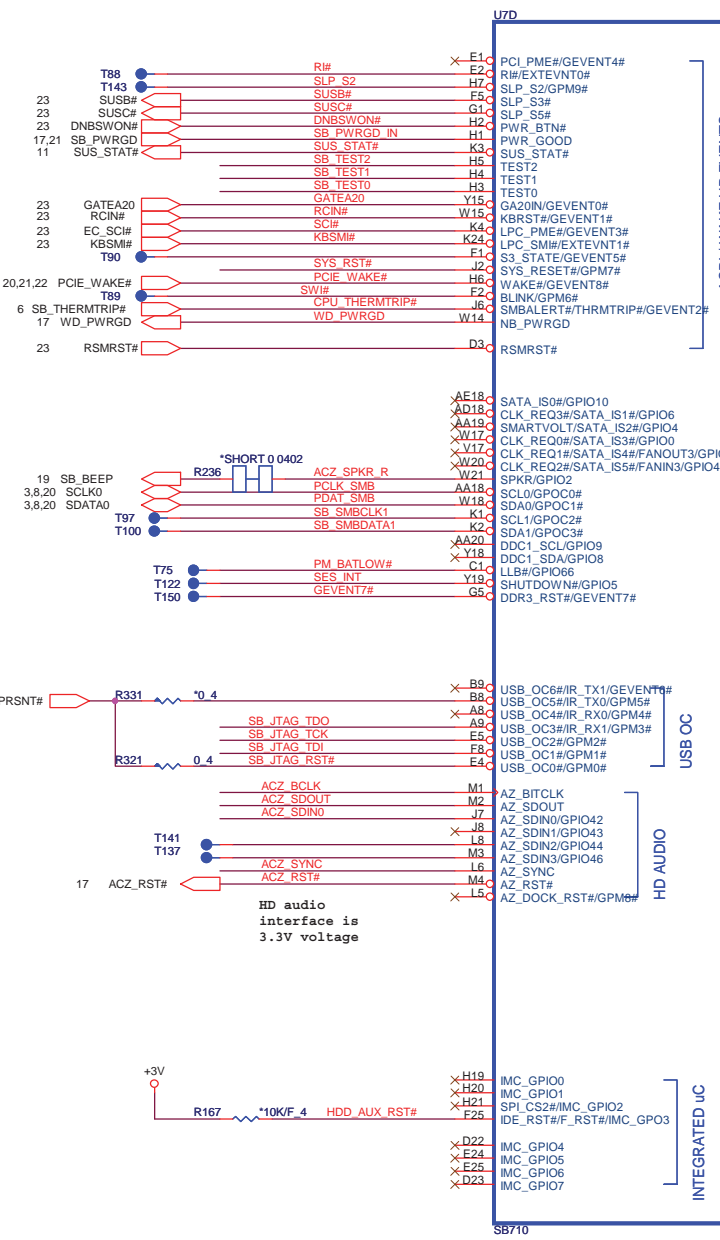
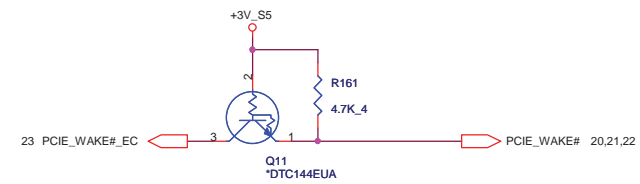
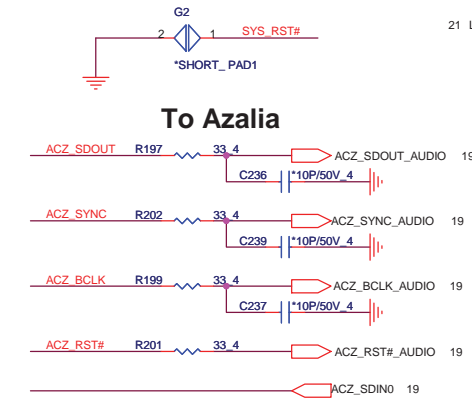
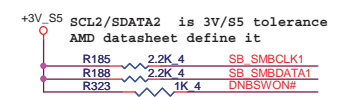
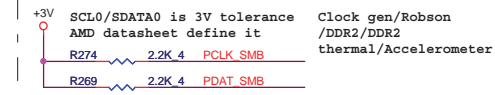
PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLTP18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDLTP18	NC	NC



PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO U600

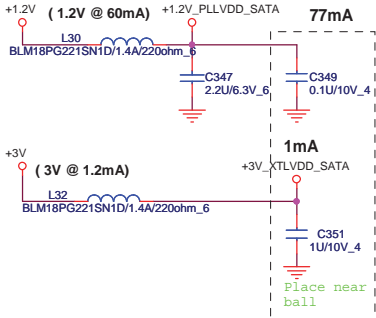
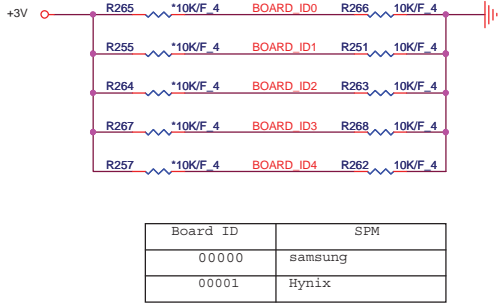
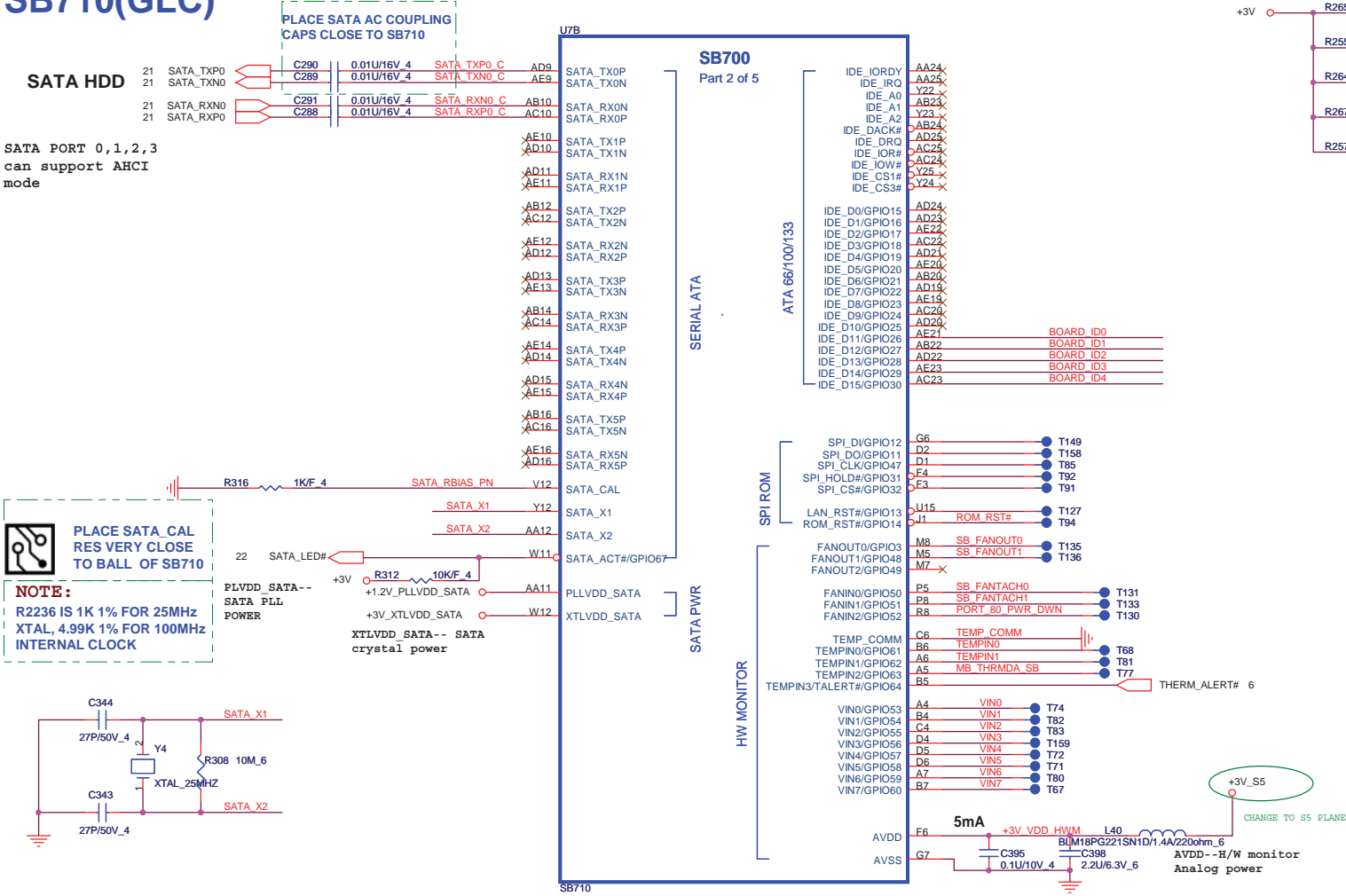


SB710(GLC)

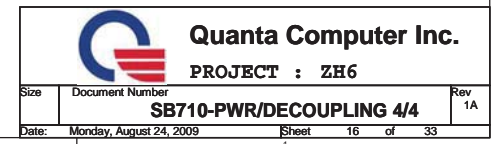




SB710(GLC)



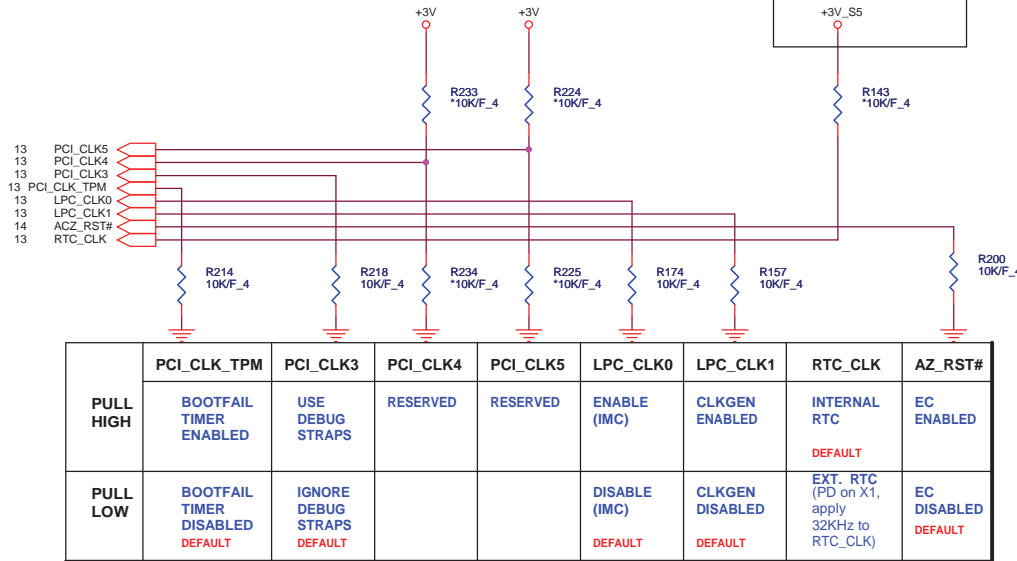




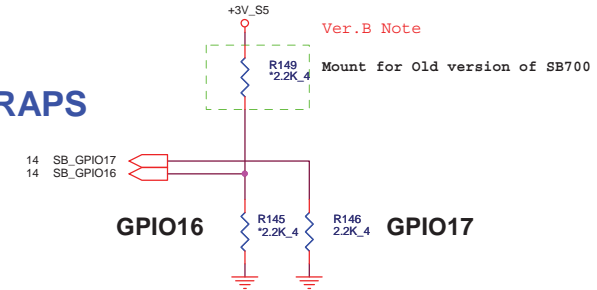


OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.

It must ready  
before RSMRST#



## REQUIRED STRAPS

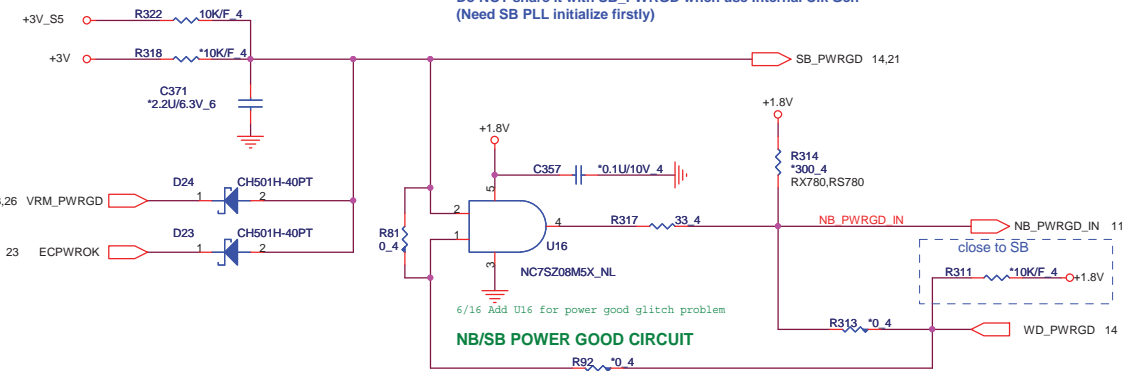
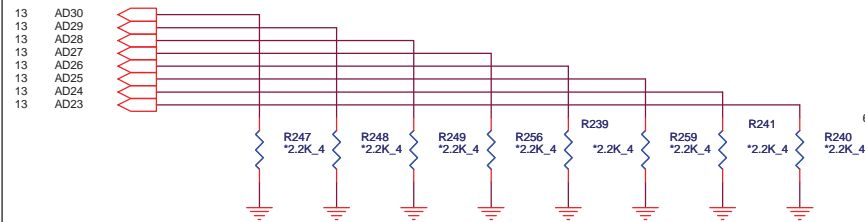


GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

## DEBUG STRAPS

SB710 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD29	PCI_AD30
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED		
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS		RESERVED	RESERVED

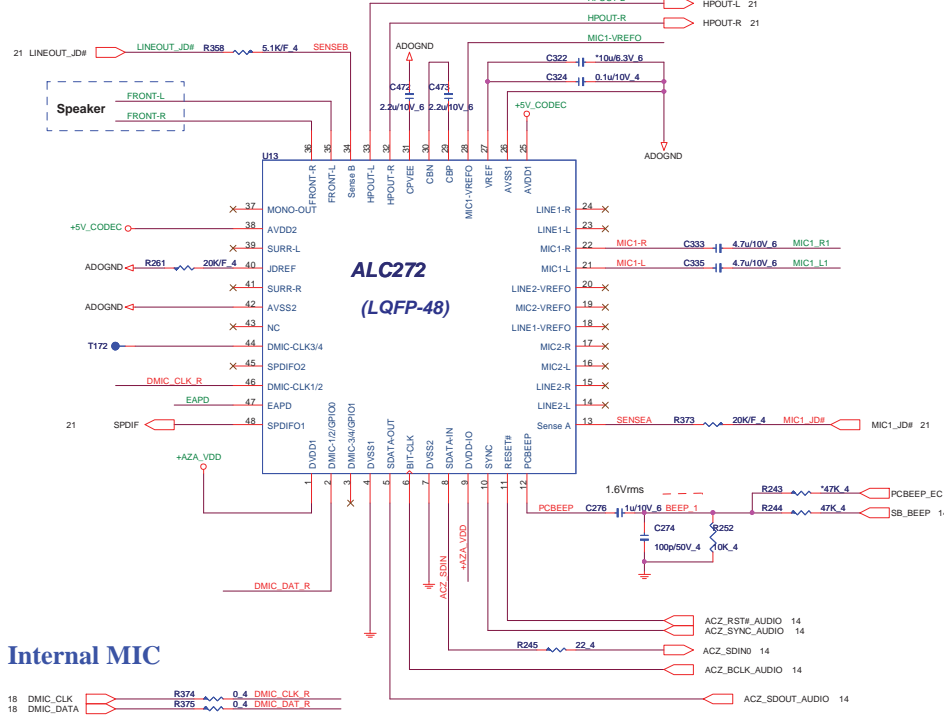
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



Quanta Computer Inc.  
PROJECT : ZH6



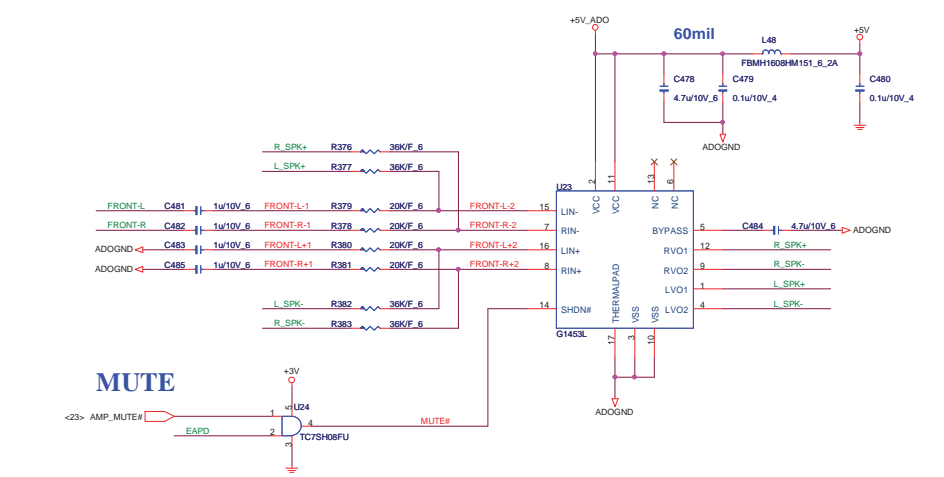
CODEC(ADO)



Internal MIC



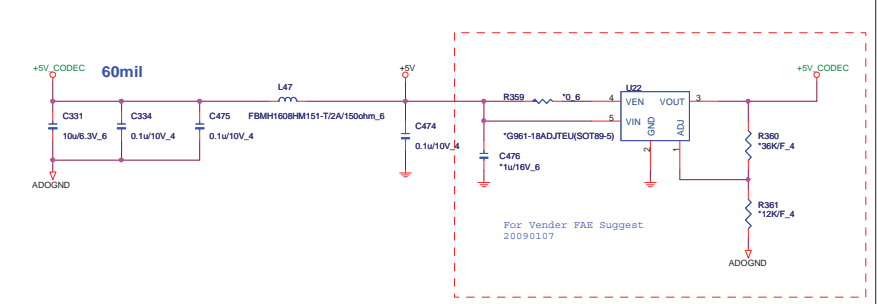
Speaker Amplifier(AMP)



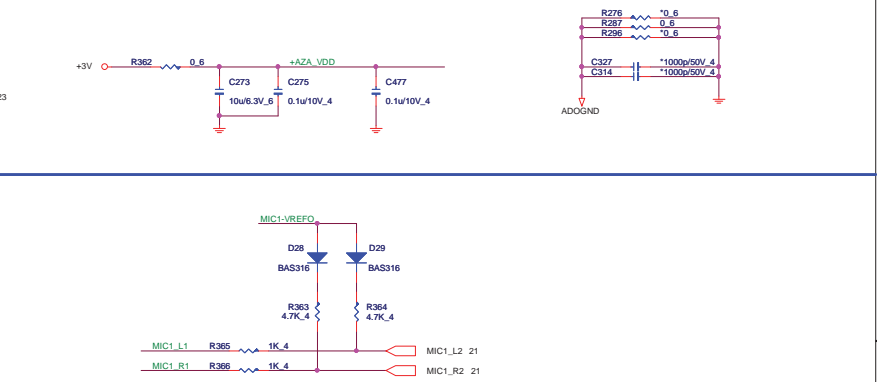
MUTE



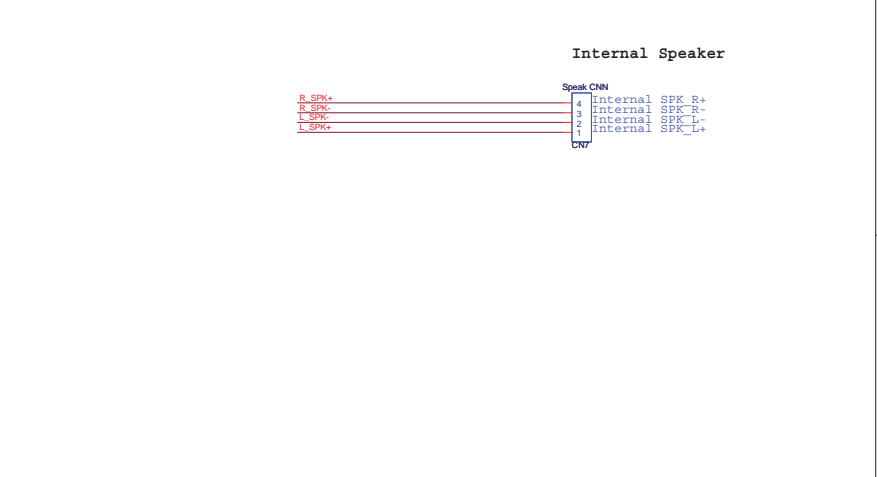
Codec Power(ADO)



HDA Power(ADO)



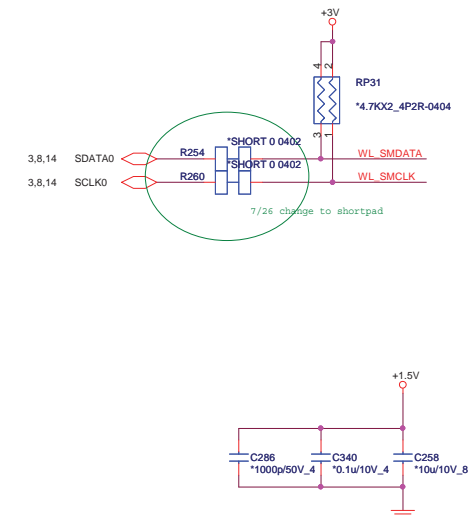
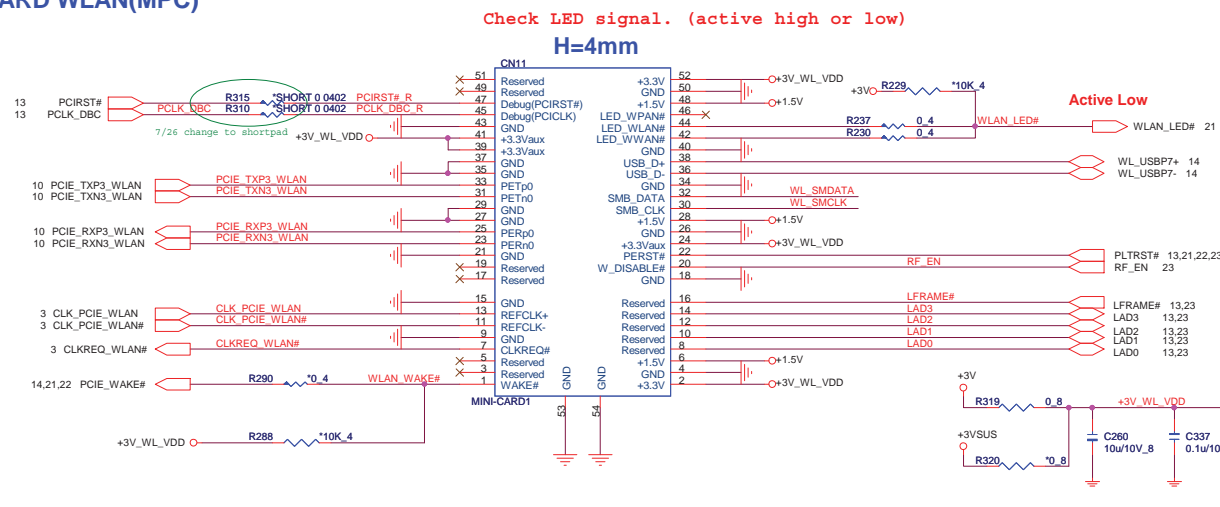
Speaker(AMP)



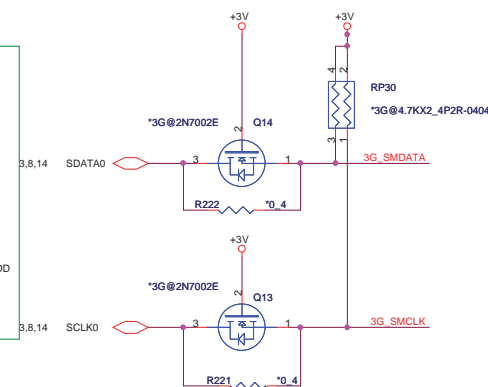
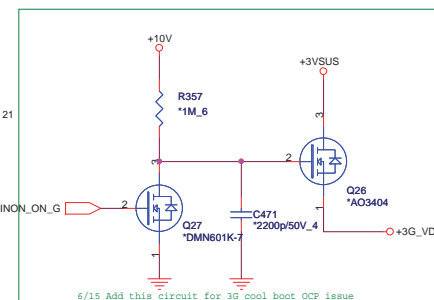
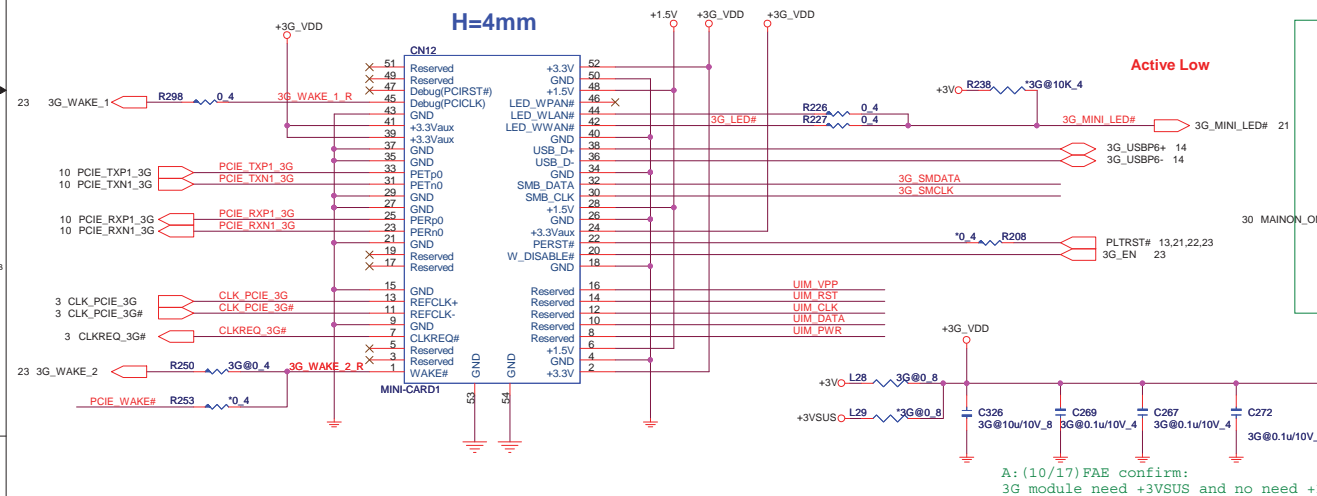
Internal Speaker



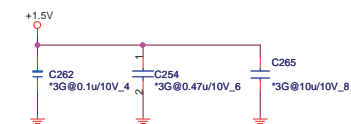
### MINI-CARD WLAN(MPC)



### MINI-CARD 3G(MNC)

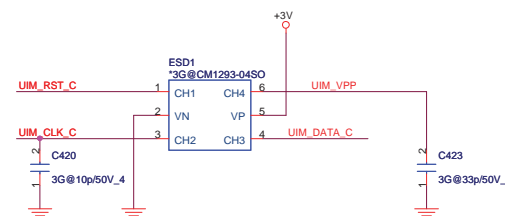
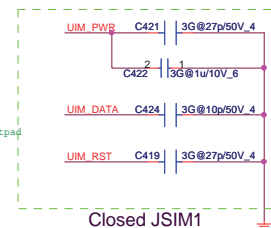
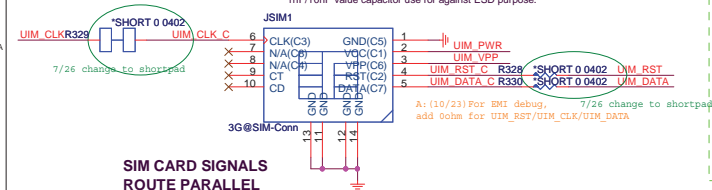



A: (10/17) FAE confirm:  
3G module need +3VSUS and no need +1.5V and no need SMBUS



### SIM CARD(RFM)

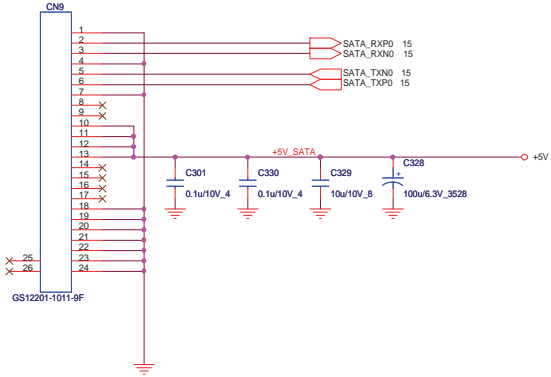
The value of the capacitor is suggest by Siemens HQ expert.  
For against 900MHz RF interference. The value of capacitor is 27pF.  
For against 1800MHz RF interference. The value of capacitor is 10pF.  
1nF/10nF value capacitor use for against ESD purpose.



 <b>Quanta Computer Inc.</b> <b>PROJECT : ZH6</b>	
Size	Document Number <b>Mini-Card/WL/3G/SIM</b>
Date	Monday, August 24, 2009 Sheet 20 of 33

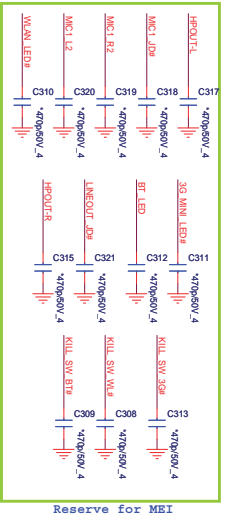
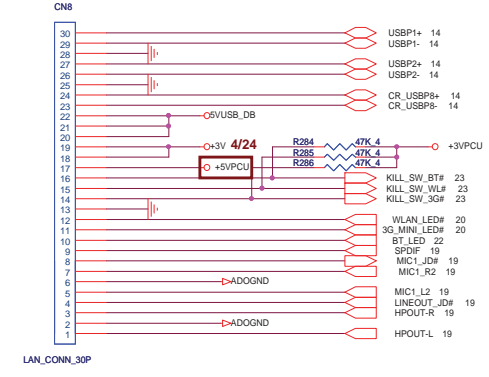
2.5" SATA HDD OR SSD(HDD)

Check SATA HDD in AVL for +3V

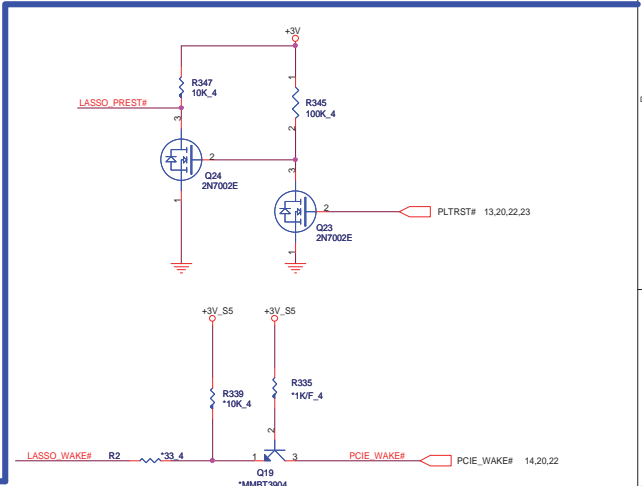


Audio, Cardreader ,Kill SW DB (AMP)

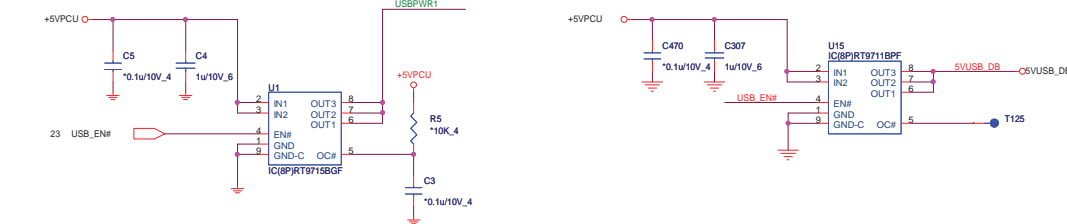
lpin=0.5A (ACES)



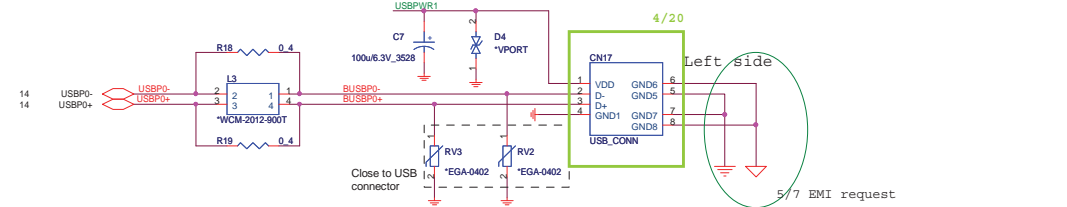
5VUSB_DB	USB_PWR	2A	2A
+3V	Card reader	250mA	275mA



(USB)

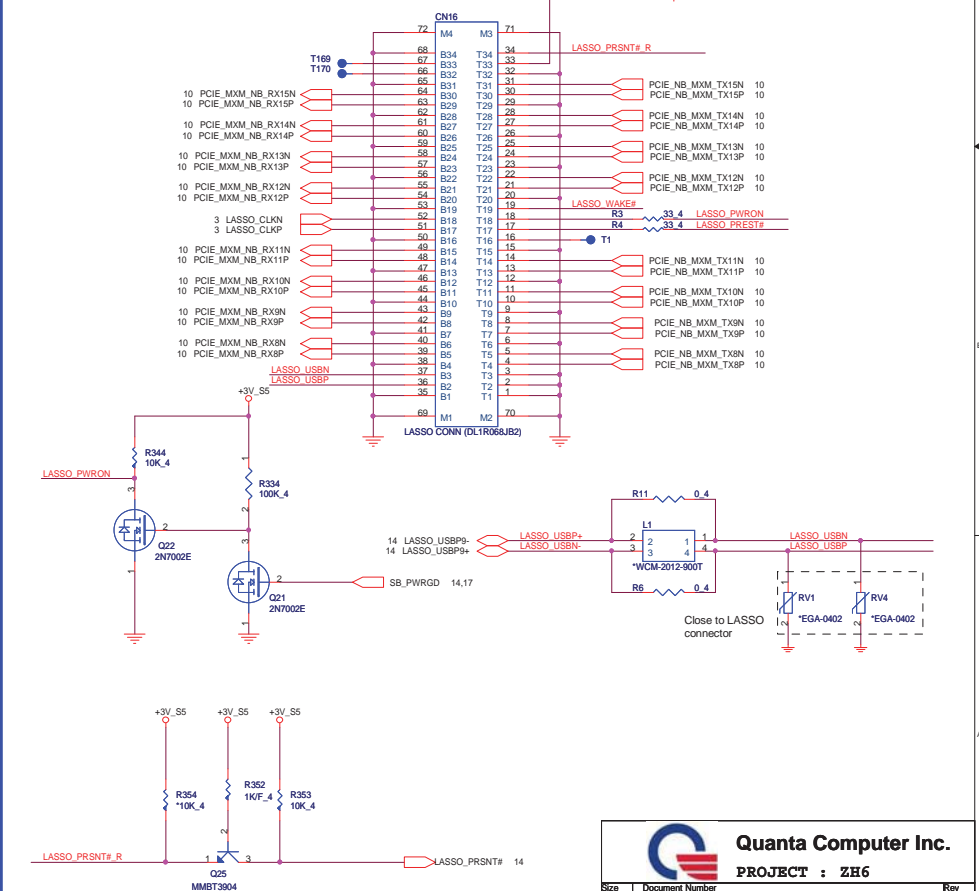


Please reserve Cin = 1uF(stuff), Cout = 10uF(don't stuff) for Richtek RT9711BPF  
Please reserve Cin = 4.7uF(stuff), Cout = 10uF(don't stuff) for GNT solution

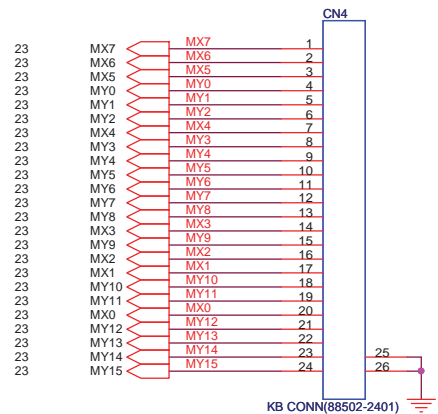


# Placed common mode chokes within 1.0" of the USB connectors

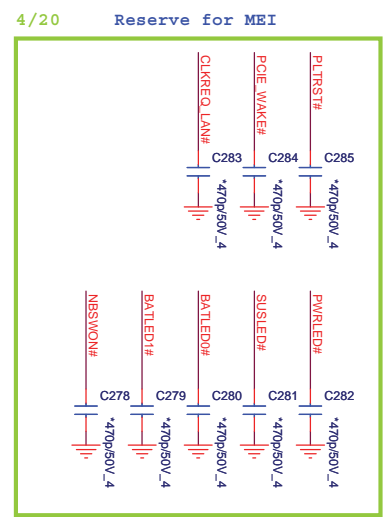
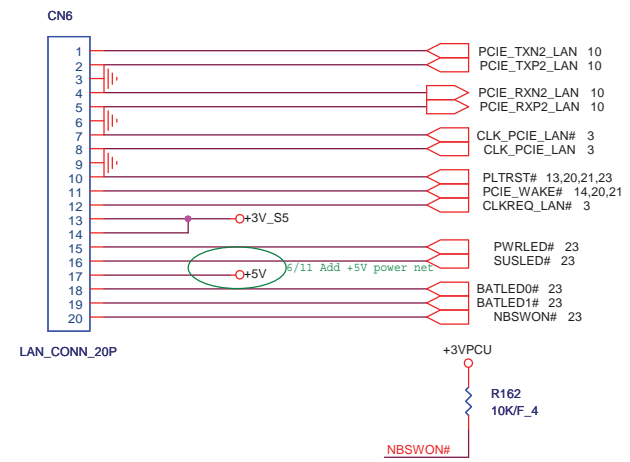
Display Port (DPP)



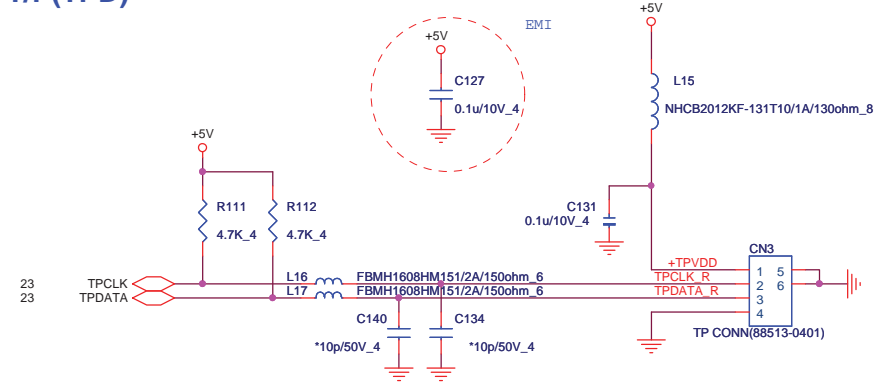
Keyboard(KBC)



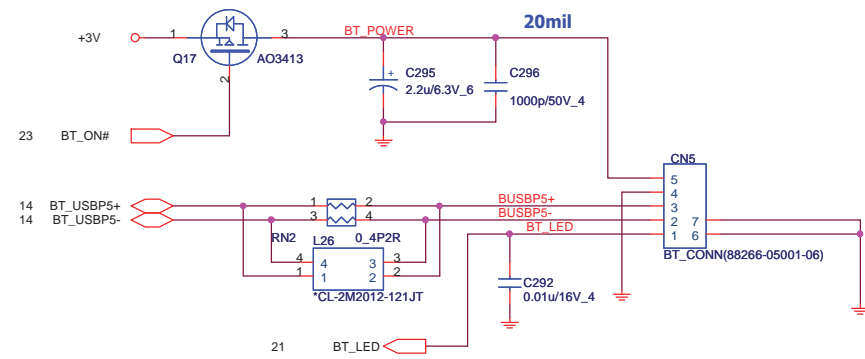
LAN , USBx2 D/B CONNECTER(LAN)



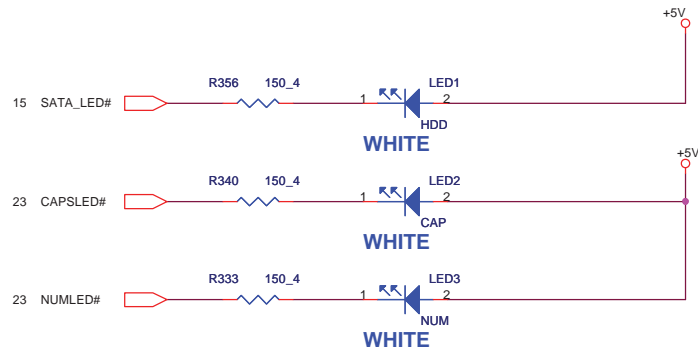
T/P(TPD)




BT(BTM)



LED(UIF)



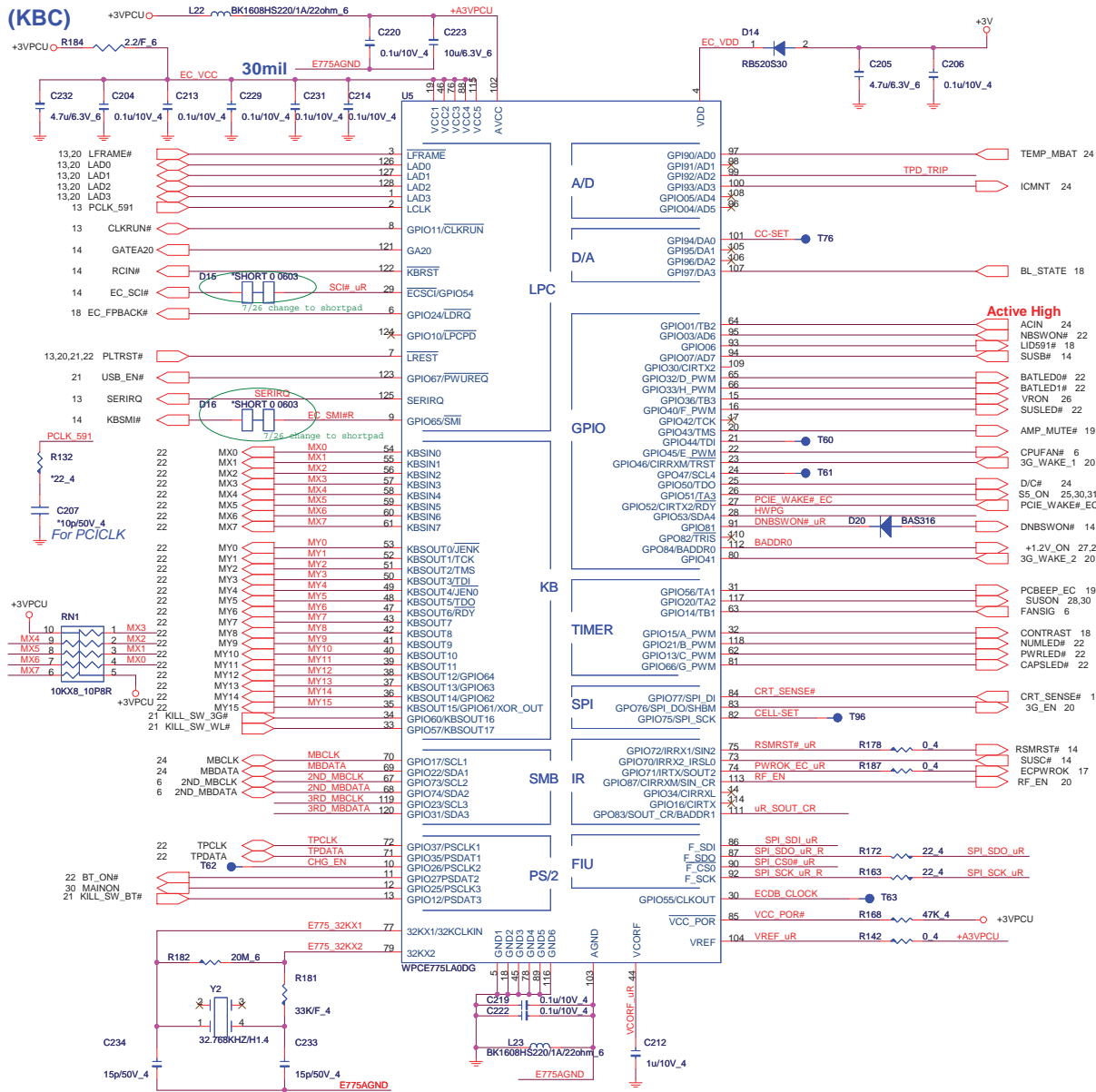


**Quanta Computer Inc.**  
**PROJECT : ZH6**

Size	Document Number	Rev
<b>TP/ USB/ KB / LED</b>		<b>1A</b>
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(KBC)



## I/O ADDRESS SETTING(KBC)

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

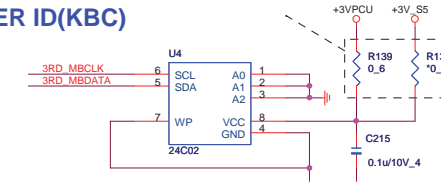


1/13 Confirm by vendor mail :  
Disabled ('1') if using FWH device on LPC.  
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

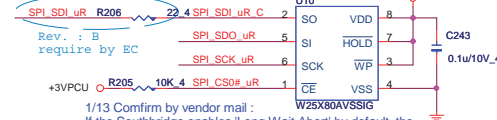
## SM BUS PU(KBC)



## ACER ID(KBC)

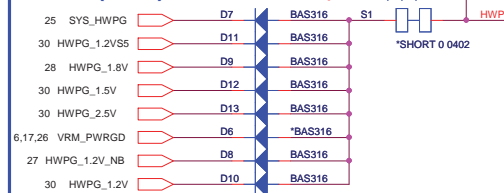


## SPI FLASH(KBC)



1/13 Confirm by vendor mail : W25X80AVSSIG  
If the Southbridge enables 'Long Wait Abort' by default, the  
flash device should be 50MHz (or faster)

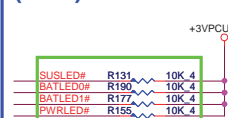
## HWPG(KBC)



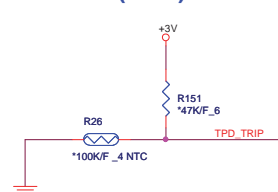
## INTERNAL KEYBOARD STRIP SET(KBC)



(KBC)



## Thermistor (THM)

**Quanta Computer Inc.**

PROJECT : ZH6

Size	Document Number <b>WPCE775L &amp; FLASH</b>		
Date	Monday, August 24, 2009	Sheet	23 of 33

# DC-IN JACK

65W Yellow DFPJ05MR007



Change footprint & P/N

C114F3-108A1-L\_Batt\_Conn

PJ2

MBAT+

TEMP\_MBAT

CDP3

PR65

0.6

RB500V-40

PC74

47p/50V\_6

PC81

0.1u/50V\_6

PR81

100\_4

PR83

100\_4

PD9

\*ZD5.6V

PD4

\*ZD5.6V

PR68

\*100K/F\_6

PC64

0.01u/50V\_6

PU4

PCM1293A-04SO

CH1

CH2

CH3

CH4

MBDATA

+3VPCU

TEMP\_MBAT\_C3

PC86

3300p/50V\_4

PC83

\*0.01u/50V\_6

PC80

0.01u/50V\_6

PC79

\*1u/16V\_6

PC84

0.01u/50V\_6

PR89

2.21K/F\_6

VCOMP

NC

ICM

ICMNT

23

PU8

ISL88731A

PGND

19

LGATE

20

PHASE

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UGATE

24

BOOT

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VDDP

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VCC

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CSSN

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CSIP

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CSIN

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CSIP

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CSIP

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CSIP

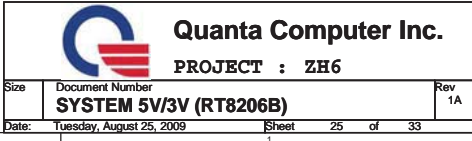
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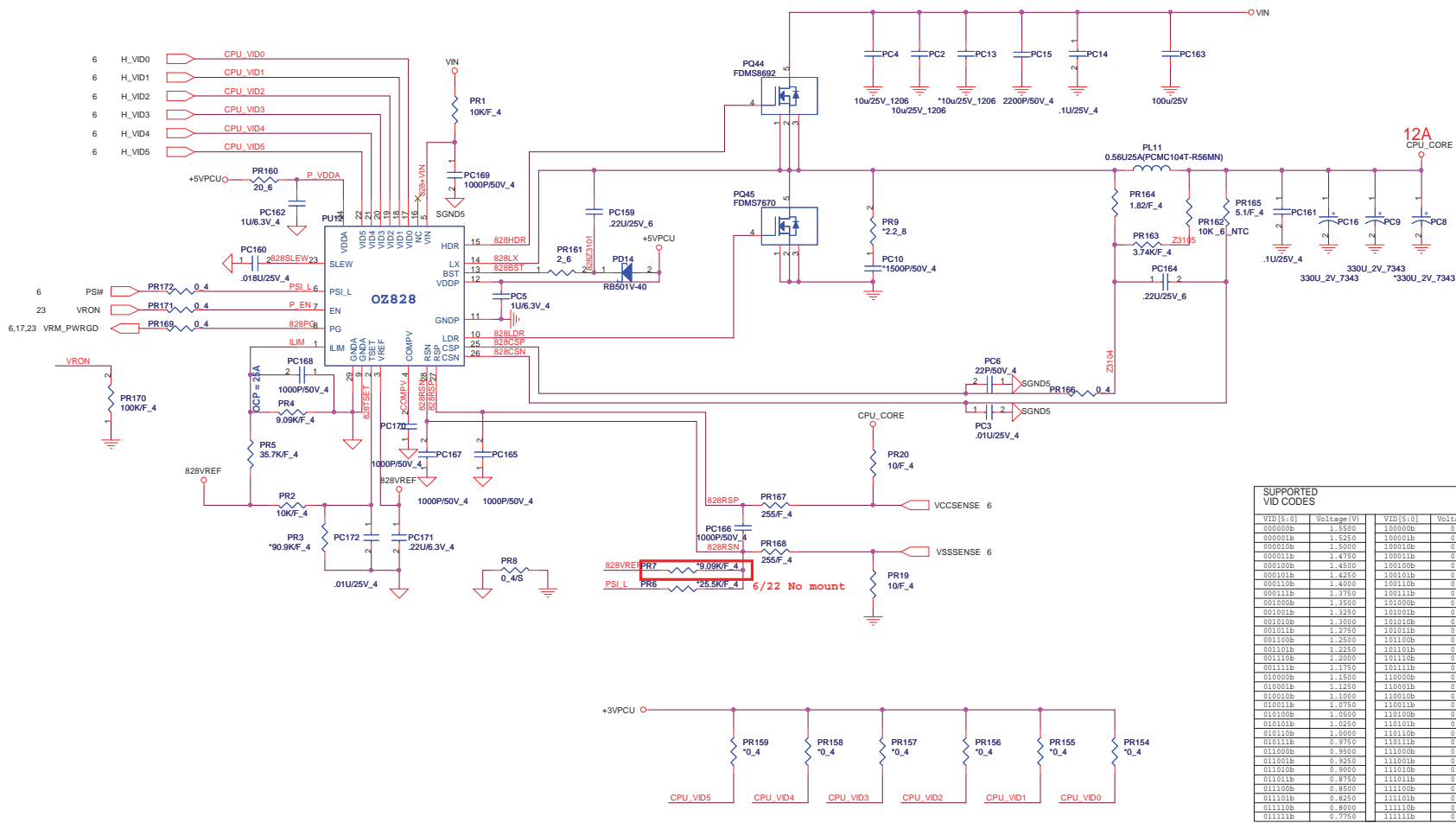
CSIP

118

CSIP

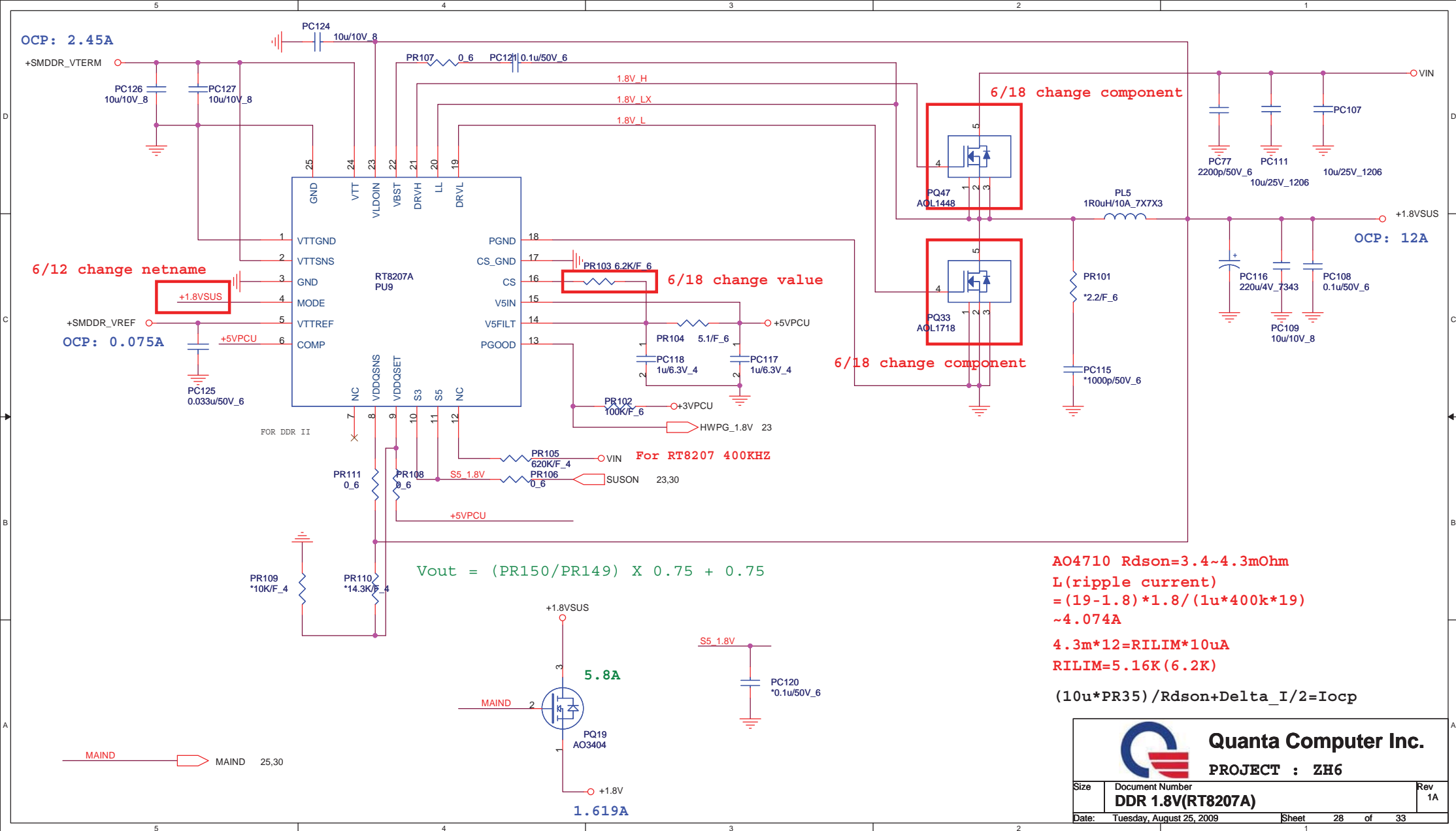
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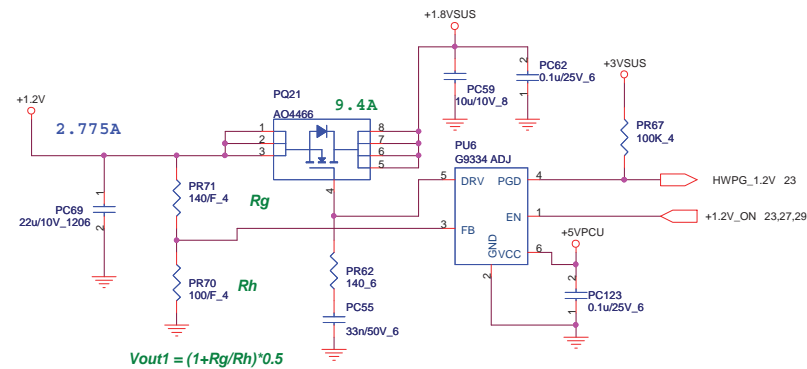
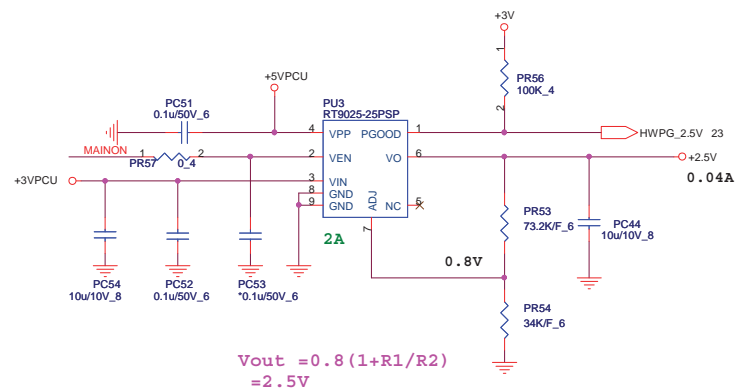
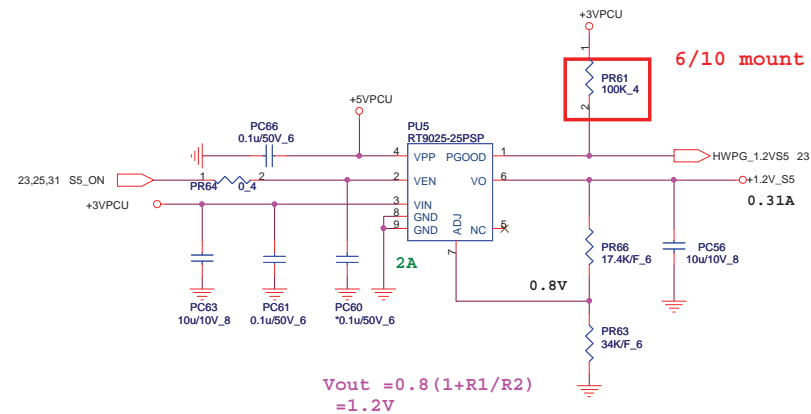
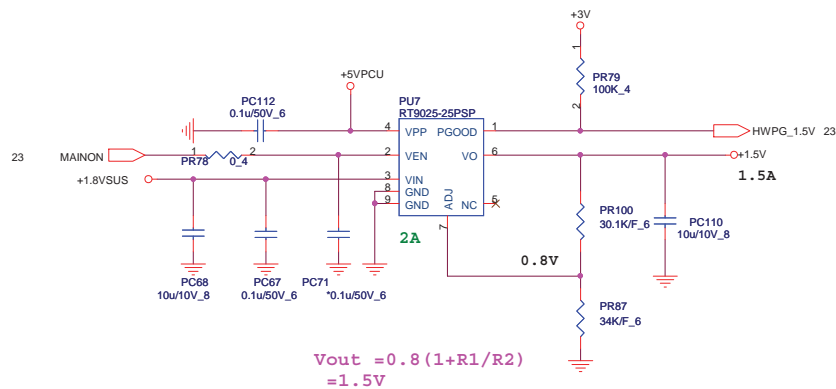
VID(5:0)	Voltage(V)	VID(5:0)	Voltage(V)
000000b	1.5500	100000b	0.7625
000001b	1.5250	100001b	0.7500
000001b	1.5000	100010b	0.7375
000010b	1.4750	100011b	0.7250
000100b	1.4500	100100b	0.7125
000101b	1.4250	100101b	0.7000
000110b	1.4000	100110b	0.6875
000111b	1.3750	100111b	0.6750
001000b	1.3500	101000b	0.6625
001001b	1.3250	101001b	0.6500
001010b	1.3000	101010b	0.6375
001011b	1.2750	101011b	0.6250
001100b	1.2500	101100b	0.6125
001101b	1.2250	101101b	0.6000
001110b	1.2000	101110b	0.5875
001111b	1.1750	101111b	0.5750
010000b	1.1500	110000b	0.5625
010001b	1.1250	110001b	0.5500
010010b	1.1000	110010b	0.5375
010011b	1.0750	110011b	0.5250
010100b	1.0500	110100b	0.5125
010101b	1.0250	110101b	0.5000
010110b	1.0000	110110b	0.4875
010111b	0.9750	110111b	0.4750
011000b	0.9500	111000b	0.4625
011001b	0.9250	111001b	0.4500
011010b	0.9000	111010b	0.4375
011011b	0.8750	111011b	0.4250
011100b	0.8500	111100b	0.4125
011101b	0.8250	111101b	0.4000
011110b	0.8000	111110b	0.3875
011111b	0.7750	111111b	0.3750



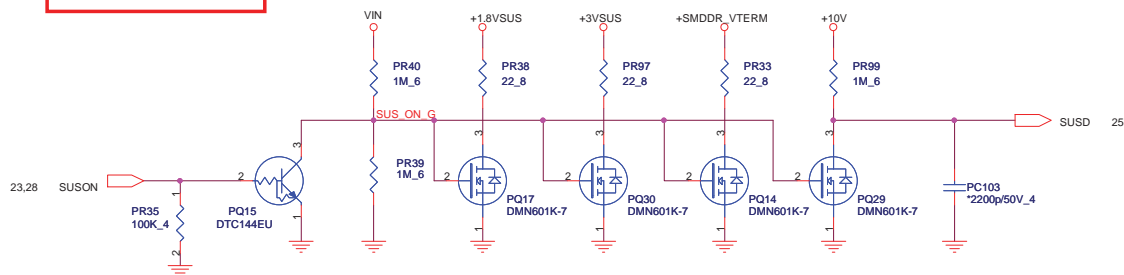




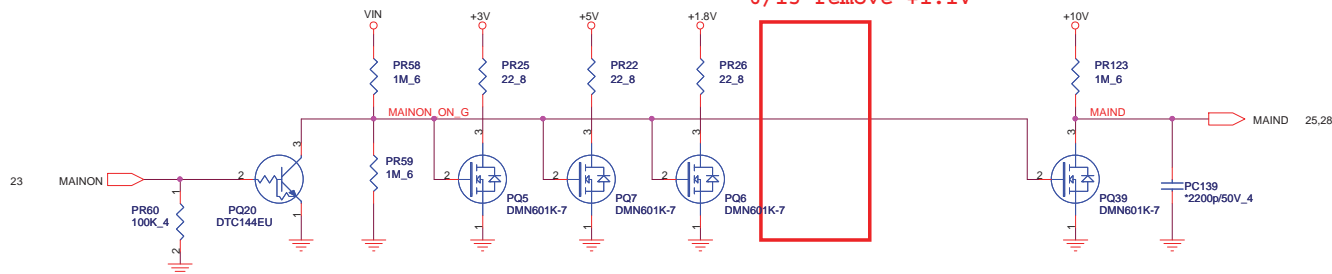


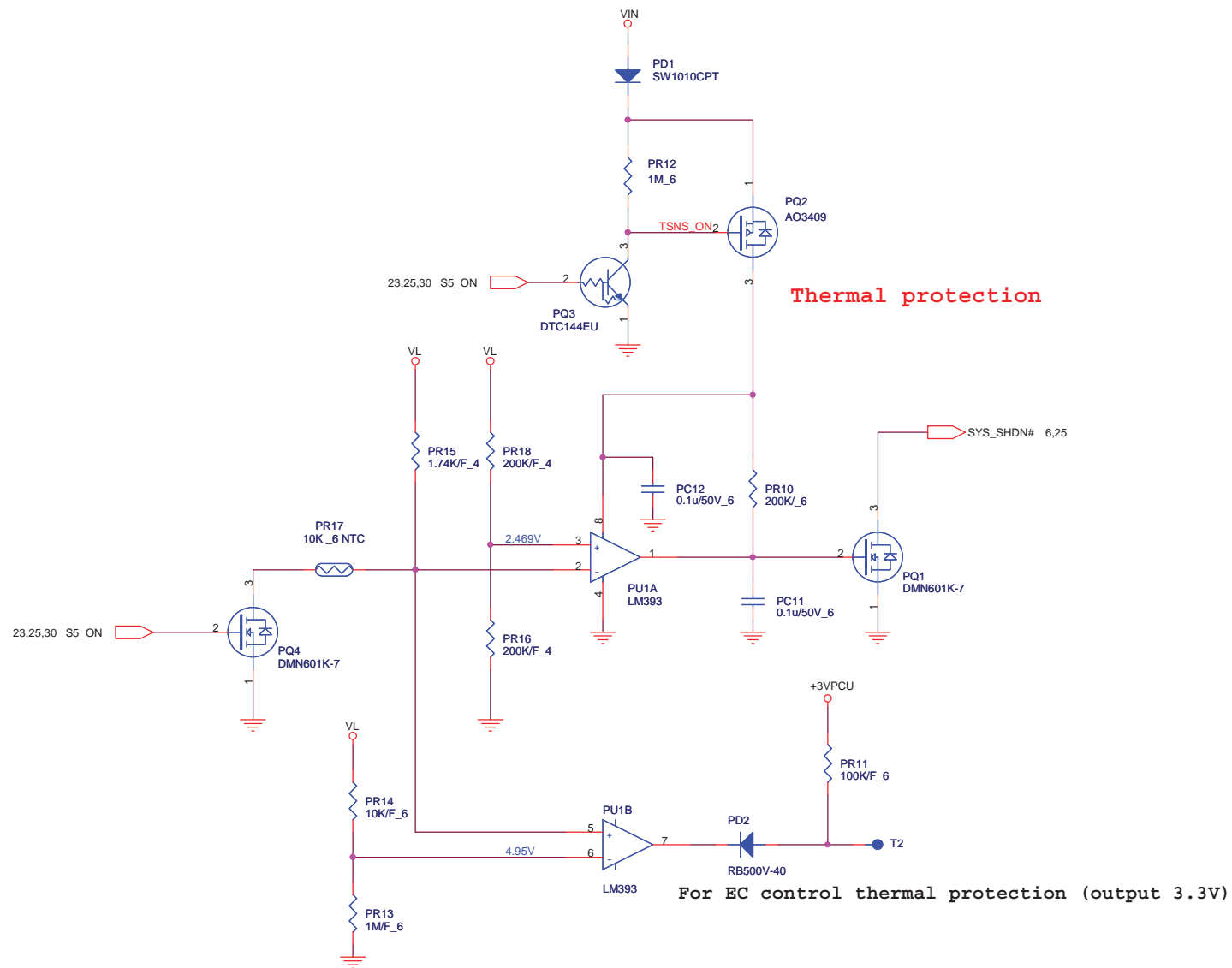


6/18 Add



6/15 remove +1.1V





Quanta Computer Inc.

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Thermal protect



PROJECT : ZH6

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Model	REV	DATE	CHANGE LIST	NOTE
ZH6		20090326	Page 30: Evan Wang add a Power source of +1.1V Page 22: add LED circuit	
		20090331	Page 3: add R5349-5356 & C32455	
		20090401	Page 20 : add LASSO circuit	
		20090402	Page 23 : remove WLAN LED and SW conn circuit Page 22 : remove LED circuit Page 19 : Change AMPLIFIER G1453L to G1431P2U circuit	
		20090403	Page 23 : add CN5021 LAN conn circuit Page 22 : Modify CN7 USB ,LAN circuit to LED , Kill SW circuit Page 18 : add HALL SENSOR circuit	
		20090406		
		20090408	Page 23 : CN4 4Pin change to 6Pin Page 08 : add CN5022 S0-DIMM circuit Page 19 : Change codec ALC272 to ALC269	
		20090410	Page 20 : Change LAN RTL8103L to AR8131 Page 20 : Change SATA CONN to 10 pin ( 85203-10021)	
		20090413	Page 23 : add CAPS,SATA,NUM LED circuit	
		20090414	Page 20 : remove LAN chip (AR8131) circuit to DB board	
		20090416	Page 18 : Change LVDS CONN CN1 Pin define Page 11 : remove R2368,R2073 Page 09 : remove C57 & change R34 to 0ohm	
		20090420	Page 21 : add EMI CAP C32554-C32562 Page 22 : add EMI CAP C32563-C32570 Page 23: add BT_SW and WL/3G_SW circuit (SW1,SW2,R5438,R5437,C79,C80,C82)	
		20090423	Page 32 : add EMI CAP PC5042-PC5049 for EMI Page 19 : modify SPDIF pin place Page 14 : modify USB port define	
		20090423	Page 21 : Modify CN7 +3VFCU to +5VFCU	
		20090427	Page 05 : add CAP C32574,C32575	
		20090429	Page 23 : remove S2 ,EC_PROCHOT ,INT LVDS DiGON&INT LVDS BLON singal Page 21: CN5024 modify pin define Page 22: change CAP ,NUM LED lamp input voltage to +3V	
		20090611	Page 12: Add C164 for VDDHTTX noise reduction Page 14: Lasso_Present reserve U7,B8 in SB	
		20090615	Page 17: Add U16 for NB_PWRGD_IN glitch issue Page 21: change HDD connector to cable type	
		20090712	Page 6: Add R104 for VRM_PWRGD pull high Page 19: Change codec to ALC272 Page 23: Change R184 to 2.2ohm for ESD solution	
		20090824	Page 32: Reserve EC1-EC6 for RF noise reduction Page 27: Add PR174 for IC BOS issue Page 29: Add PR175 for IC BOS issue	